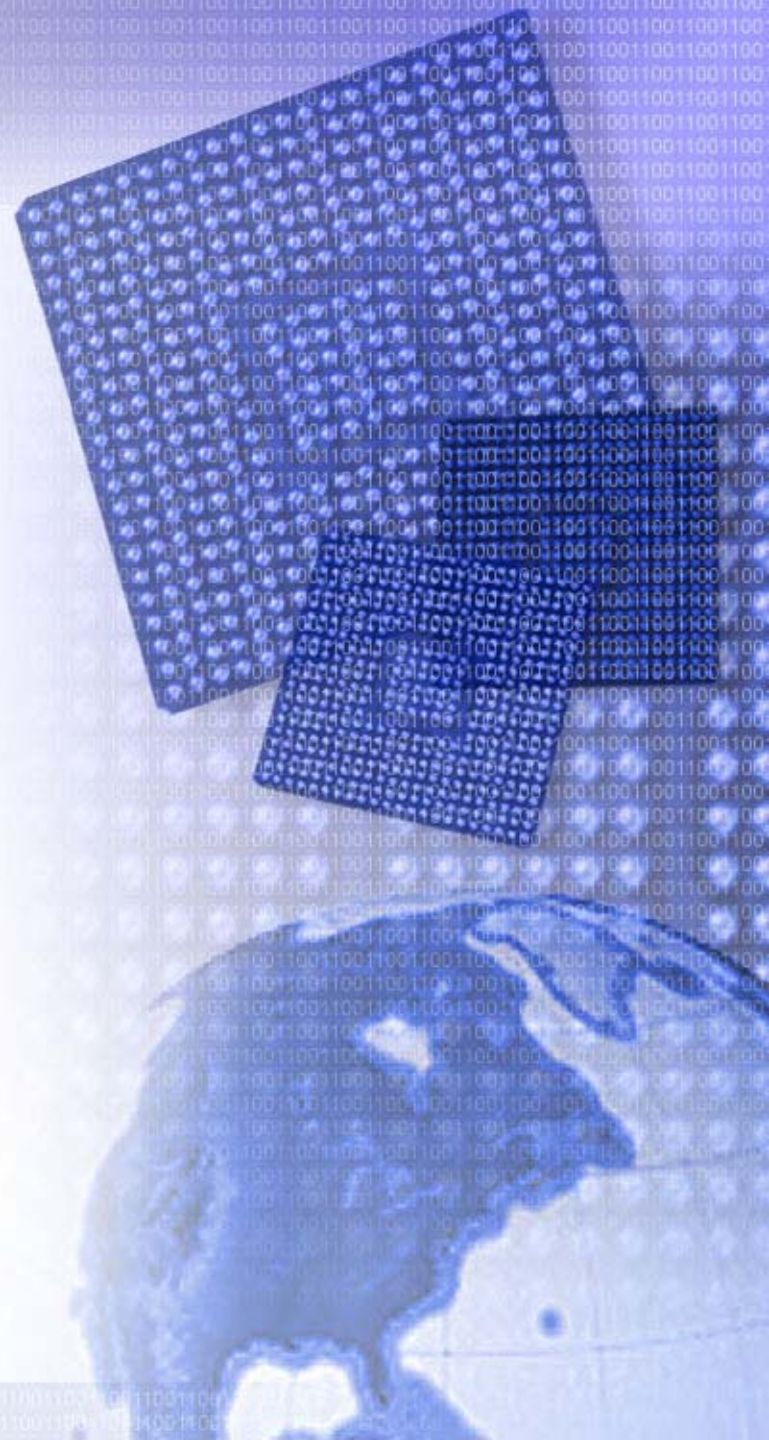




SONET / SDH



Agenda

- Introduction
- Market Data, Dynamics and Analysis
- SONET Architecture
- SDH
- SONET/SDH Equipment
- Competing Technologies
- Xilinx Solutions
- Summary



Introduction



What is SONET/SDH?

- Both SONET and SDH are standards for a synchronous, fiber-optic transport system
- SONET, or Synchronous Optical NETWORK, is the North American standard
- SDH, or Synchronous Digital Hierarchy, is the similar standard used in the rest of the world
- SONET works at Layer 1 (Physical) OSI-RM
- SONET/SDH's strength is in transporting delay sensitive voice and video, but are also used for high speed data transport

Benefits of SONET/SDH

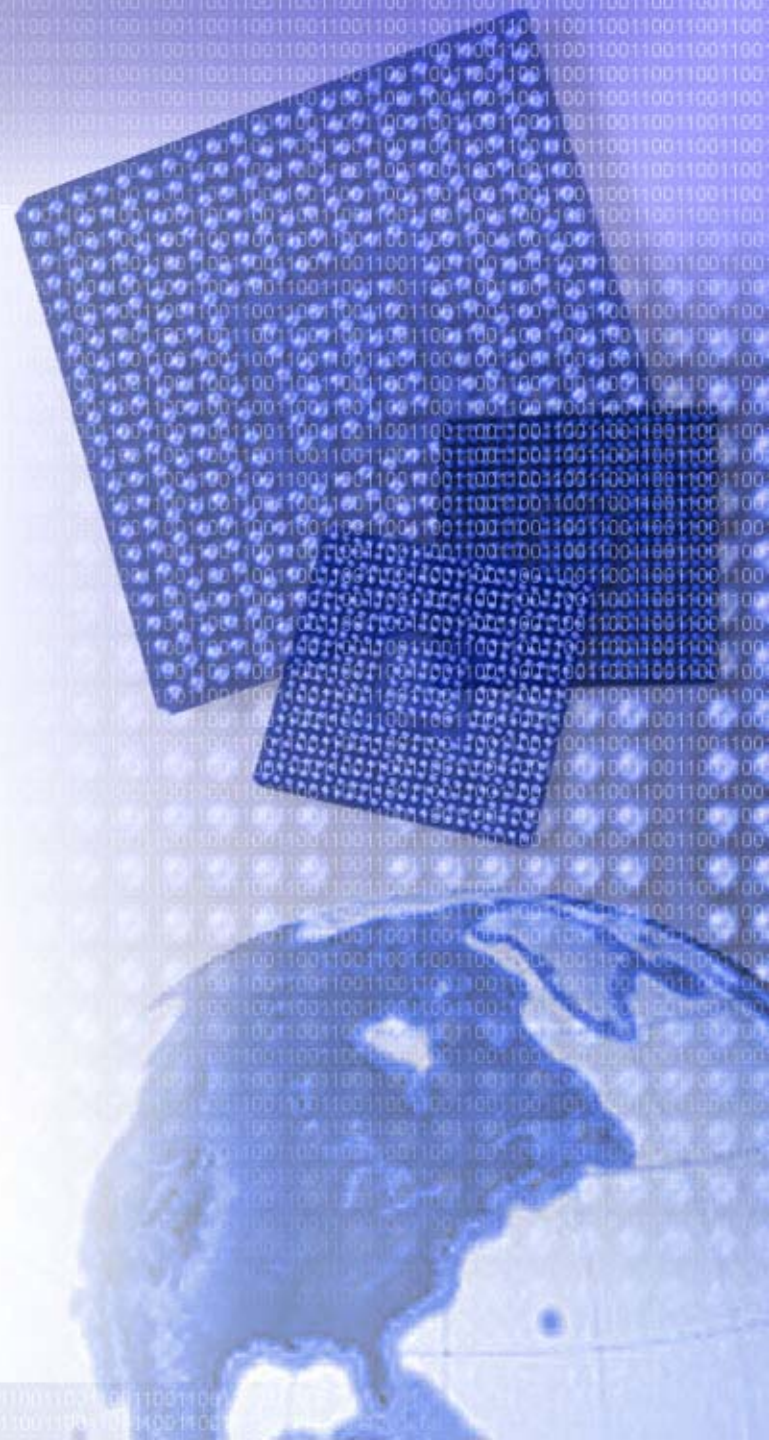
- Standardization
- High Speed
- Reliability
- Operations, Administration, Maintenance & Provisioning (OAM & P)
- Quality of Service (QoS)
- Flexibility
- Scalability

SONET/SDH Supports

- Applications
 - Voice
 - Digital Cable
 - Broadband access
 - Internet
 - Interoffice trunking
 - Private backbone networks
 - MANs and WANs
 - Cellular PCS cell-site transport
 - And many more
- Technologies
 - TE-carriers
 - ATM transport
 - Packet over SONET
 - Frame Relay access



Market Data, Dynamics, and Analysis



Why SONET/SDH?

- Need for a digital transmission system faster and more sophisticated than T-E systems
 - International telecommunications committees anticipated that growth in high bandwidth applications would require more capacity than that provided by current TE carrier technology
- Equipment interoperability, or “mid-span meet”
 - “Mid-span meet” issue was highlighted after AT&T divestiture and declaration of “equal access rights”
 - Telcos could connect their equipment to AT&T's local switches, but frequently not interoperable

History of SONET/SDH

- 1984 - MCI raises “mid-span meet” issue to various standards bodies
 - Interexchange Carrier Compatibility Forum (ICCF), Bellcore (Now Telecordia), ANSI, and CCITT (now ITU-T)
- 1985 - Bellcore proposes conceptual foundation; ANSI drives efforts
 - 400 technical proposals from 120 people from 50 companies
- 1986 - ITU-T begins effort for European version of SONET called SDH
- 1987 - ITU-T rejects T1X1s proposal due to being T-carrier (US) biased
 - SONET 50 Mbps base rate not useful for 139 Mbps E-4 signal

History of SONET/SDH

- 1988 - T1X1 proposal meets rest of the world approval
 - E-4 transport possible with definition of the SDH base rate as 155.52 Mbps
- 1990 - Operation of Multi-vendor SONET network at OC-1 and OC-3
- Three Phase process
 - Phase I: Addressed issue of passing bits between two equipment (1988)
 - Phase II: Addressed issue of multivendor interoperability (1990/91)
 - Phase III: Addressed issue of OAM&P (still ongoing)

SONET/SDH Today

- SONET/SDH technology in 95% of Service Provider high-speed, worldwide networks
 - AT&T, MCI Worldcom, Qwest, SBC, Sprint, US West, etc.
- Multiple, global equipment makers
 - Alcatel, Cisco, Fujitsu, Lucent, Marconi, Nortel, Tellabs, etc.
- Performance continues to increase
 - OC-48 widely deployed; OC-192/768 emerging

Factors affecting SONET/SDH

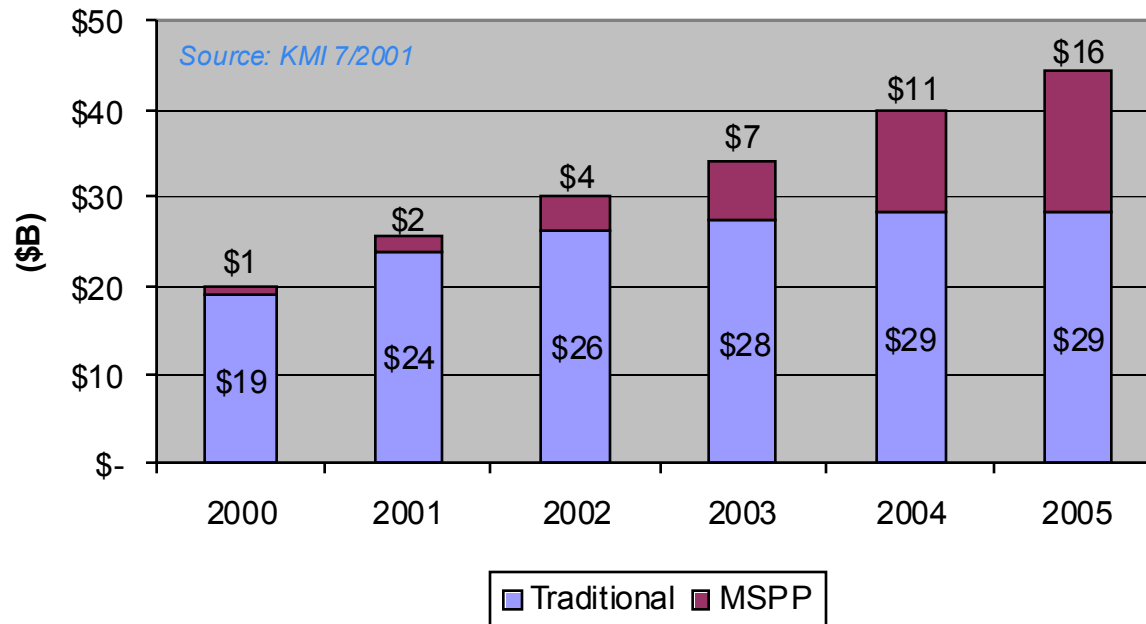
- Increase in Data Communications traffic
 - Data traffic is 2 times voice traffic
- Too many equipment w/ variety of traffic
 - ADM, DCS, Ethernet switch, ATM switch, IP switch/router, DWDM transport terminal
- Carriers want to address the above issues while keeping the benefits of SONET
 - Standardization, Reliability, Flexibility, QoS, and Manageability, Scalability

Future of SONET/SDH

- Faster speeds on legacy SONET equipment
 - OC-768 coming to market; OC-3072 in the works
- Proliferation to the Edge, MAN and WAN
- Multi-Service Provisioning Platforms (MSPP)
 - MSPPs are SONET/SDH equipment geared for data transport
 - Combines various functionality into one chassis
 - SONET equipment (I.e. ADMs and DCSs) + non-TDM functionality (IP and Layer 2 switching, DWDM)
 - Built for the Metro Edge Networks to alleviate metro-bottleneck, save rack space, power, and \$\$\$

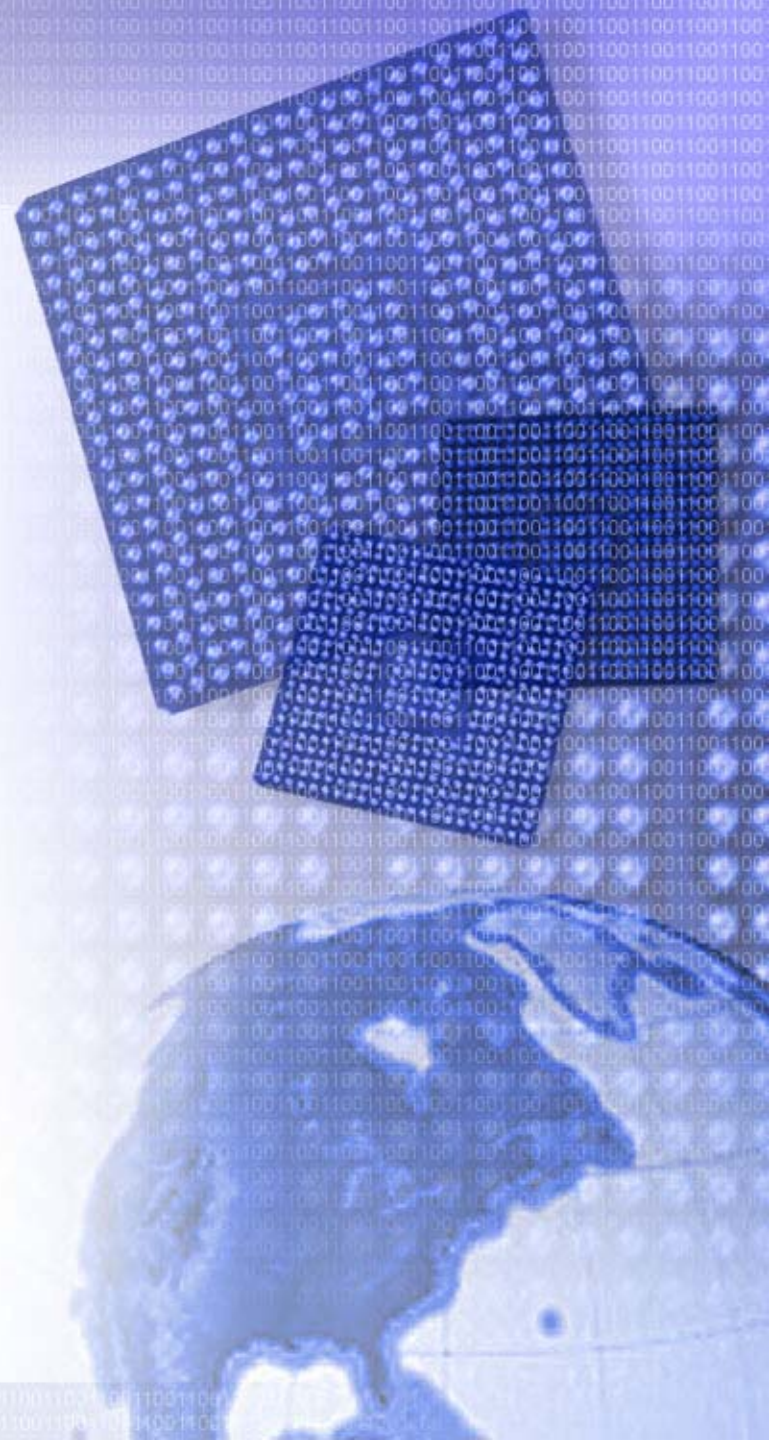
Market Estimate - Equipment

- Multi-Service SONET/SDH to grow at the expense of traditional SONET/SDH
 - MSPP Forecast for 2005: \$16 B (out of \$45 B)





SONET Architecture

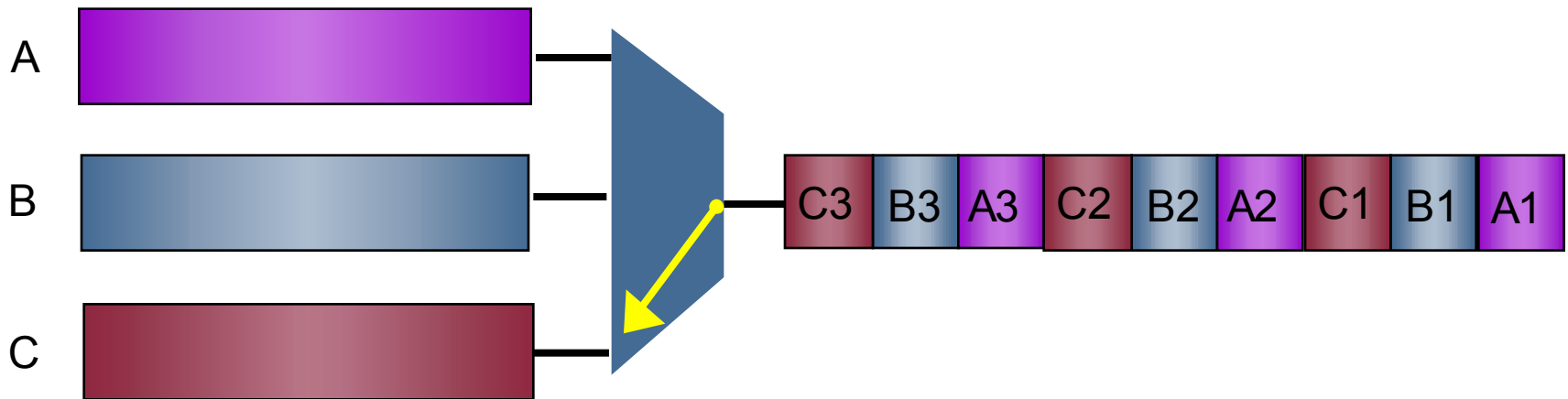


Topics

- Time Division Multiplexing (TDM) and Pulse Code Modulation (PCM)
- Multiplexing Hierarchy and Line Rates
- SONET Frame Architecture
- SONET Overhead
- SONET Synchronization
- Payload Types

Time Division Multiplexing

- Slow-rate bitstreams combined into a fast-rate bitstream
- Done by taking samples from each bit stream ,in round-robin fashion, at a fixed rate
- Constant flow of data; not “bursty” like Ethernet

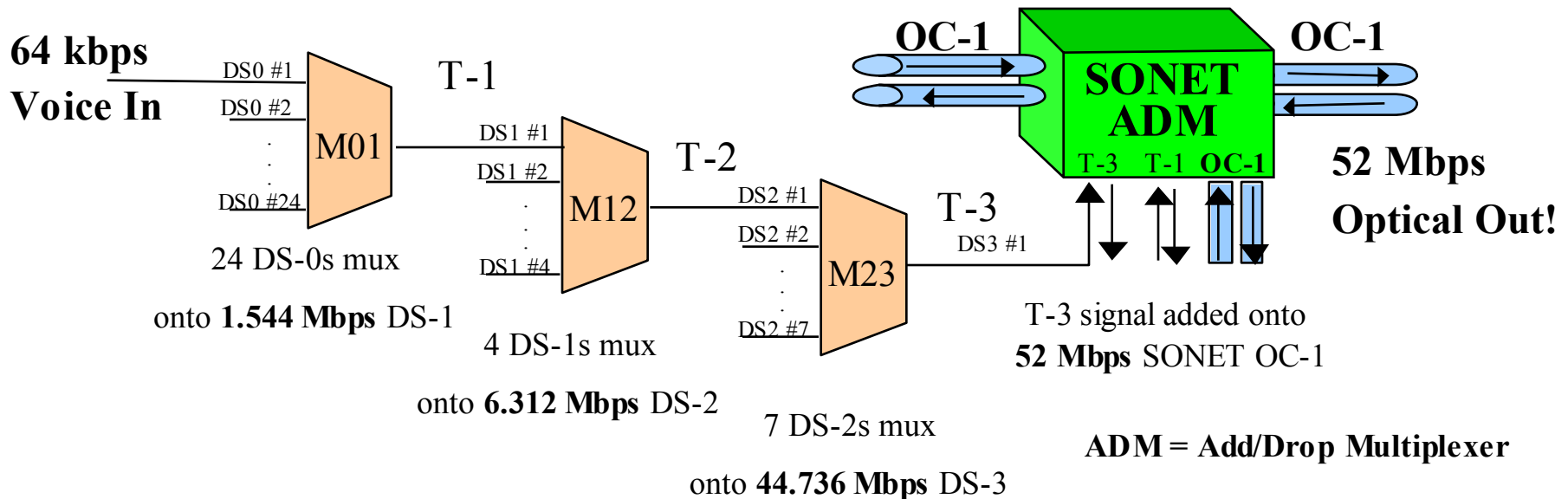


Pulse Code Modulation of Voice

- PCM involves sampling a 4 khz voice channel at twice the frequency, i.e. 8000 samples per second (Nyquist's Rule)
- Each sample is encoded into 8 bits
- Therefore need 64 kbps (8×8000) for each voice channel!
 - This base level for the digital hierarchy is called DS0
- How does your DS-0 voice channel get onto a SONET signal?

From Voice to SONET

- SONET starts off where TE carriers leave off!
- Sequentially increasing Time Division
 - **DS-0 voice** => **DS-1** => **DS-2** => **DS-3** => **SONET OC-1**



SONET Line Rates

- Hierarchy of line rates
 - Various rates for transferring SONET “frames” in the Optical and Electrical domains
- Faster signals are integer multiples of STS-1, i.e. STS-N
- Popular rates are OC-3, OC-12, OC-48, & OC-192

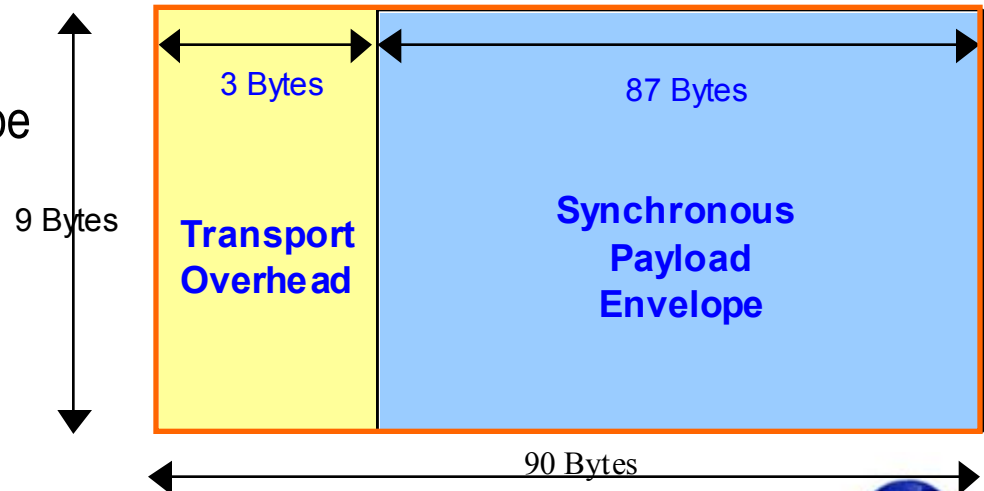
Electrical	Optical	Line Rate
STS-1	OC-1	51.84 Mbps
STS-3	OC-3	155.52 Mbps
STS-9	OC-9	466.56 Mbps
STS-12	OC-12	622.08 Mbps
STS-18	OC-18	933.12 Mbps
STS-24	OC-24	1.2 Gbps
STS-36	OC-36	1.9 Gbps
STS-48	OC-48	2.5 Gbps
STS-96	OC-96	5 Gbps
STS-192	OC-192	10 Gbps
STS-768	OC-768	40 Gbps
STS-3072	OC-3072	160 Gbps

STS = Synchronous Transport Signal

OC = Optical Carrier

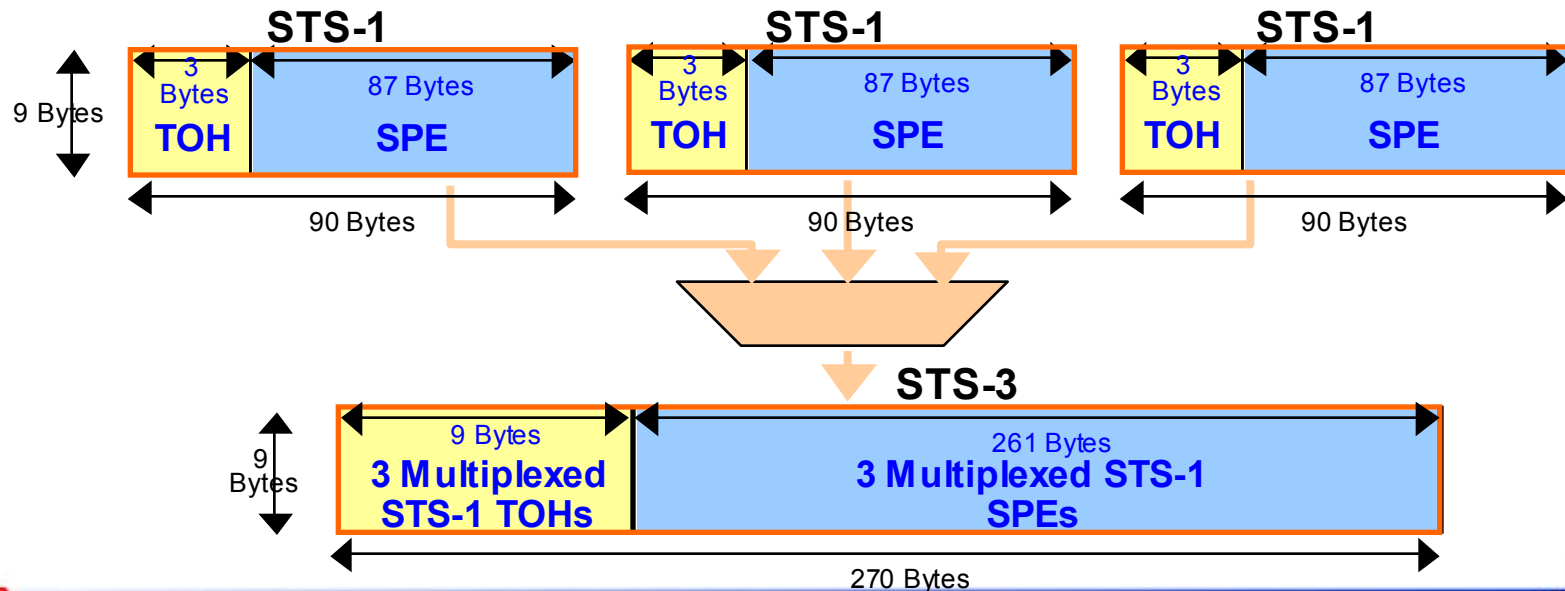
Basic Frame: STS-1

- 2-D, Byte-interleaved (9 x 90 = 810 bytes)
 - 2-D because 1-D representation would be too wide
- 2 Main components:
 - Transport Overhead (TOH)
 - Synchronous Payload Envelope (SPE)
- Transmit Row-by-Row, Top-to-Bottom, Left-to-Right
- An STS-1 gets sent every 125 μ S => 51.84 Mbps
 - Specifically intended to transport a 45 Mbps DS-3 signal



STS-N Frames

- STS-N frames are formed by byte-interleaving lower rate STS modules
 - 3 STS-1 are muxed to create an STS-3 (156 Mbps)
 - Have 3 sets of TOHs and 3 SPEs.

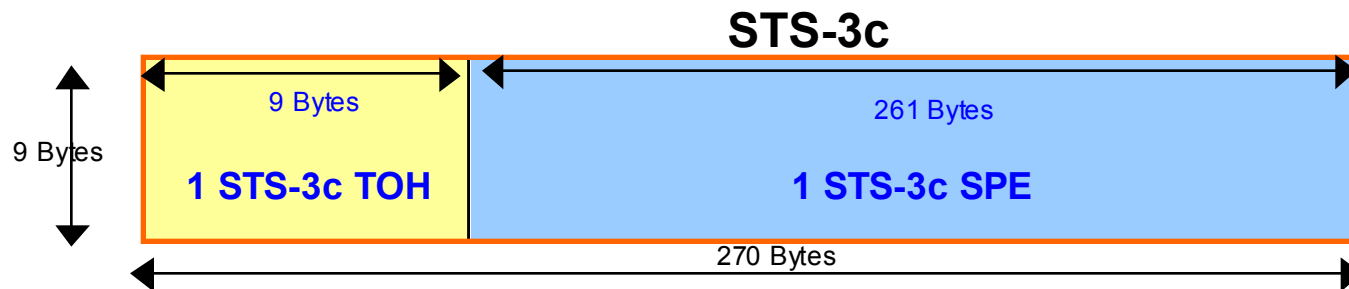


Concatenated Frames (STS-Nc)

- Concatenated STS-N frames are called as STS-Nc where “c” denotes concatenation
- Also called a “super-rate” payload
- Instead of multiple slow rate SPEs combined into one SPE, have 1 high-capacity and “unchannelized” SPE
- Useful for sending traffic that is bigger than STS-1 payload

STS-3c Frame

- For example, an STS-3c provides the full 156 Mbps rate rather than 3 channels of 52 Mbps STS-1s
 - For high bit rate channels like an E-4 (139 Mbps)
 - One TOH and one SPE
- Slowest concatenated signal is STS-3c
 - Create higher order STS-Nc signals from STS-3c



STS-3 vs. STS-3c

- Non-concatenated STS-3

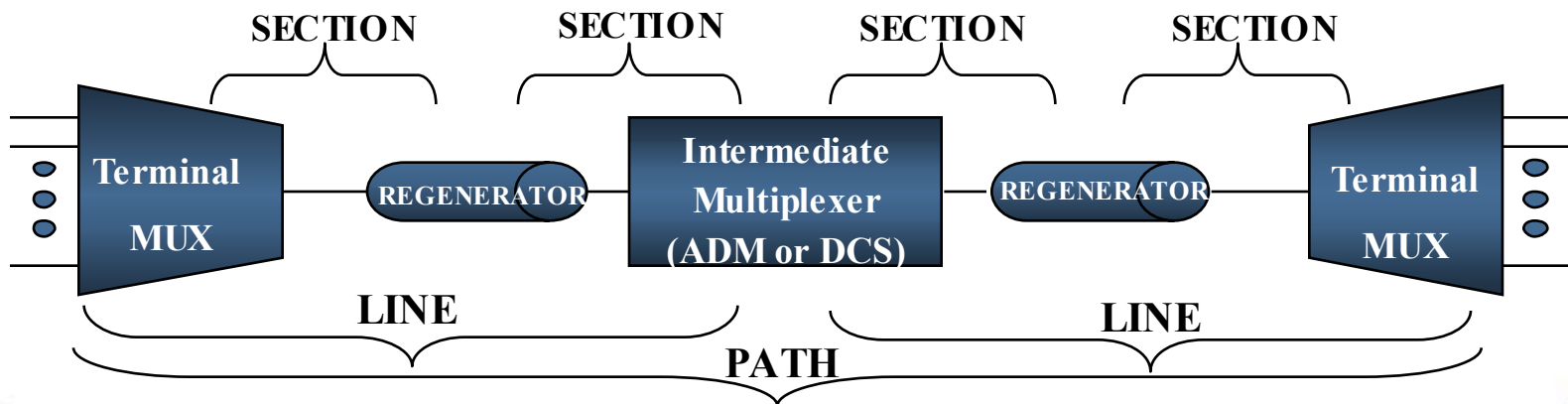


- Concatenated STS-3c

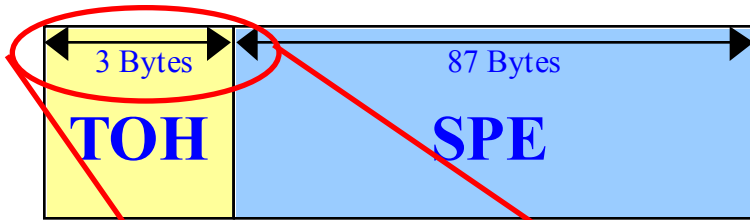


SONET Overhead

- Substantial overhead for muxing and better OAM&P
- Network Elements (NE)
 - Terminal Mux
 - Intermediate Mux
 - Regenerator
- 3 layers of overhead
 - Path Overhead (POH)
 - end to end transport
 - Line Overhead (LOH)
 - Mux to Mux transport
 - Section Overhead (SOH)
 - adjacent NE transport



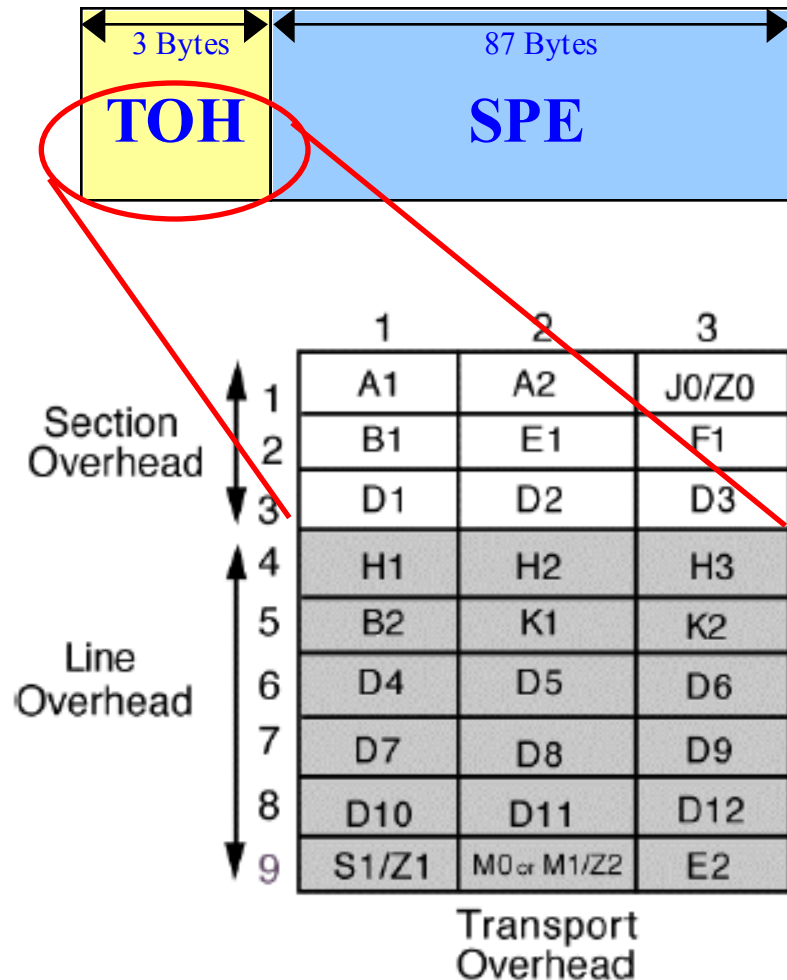
Section Overhead



- 1st 3 rows of the TOH
 - 9 Bytes
- Main functions
 - Monitor STS-N Performance
 - Local Orderwire
 - Data communication channels for OAM&P info
 - Framing

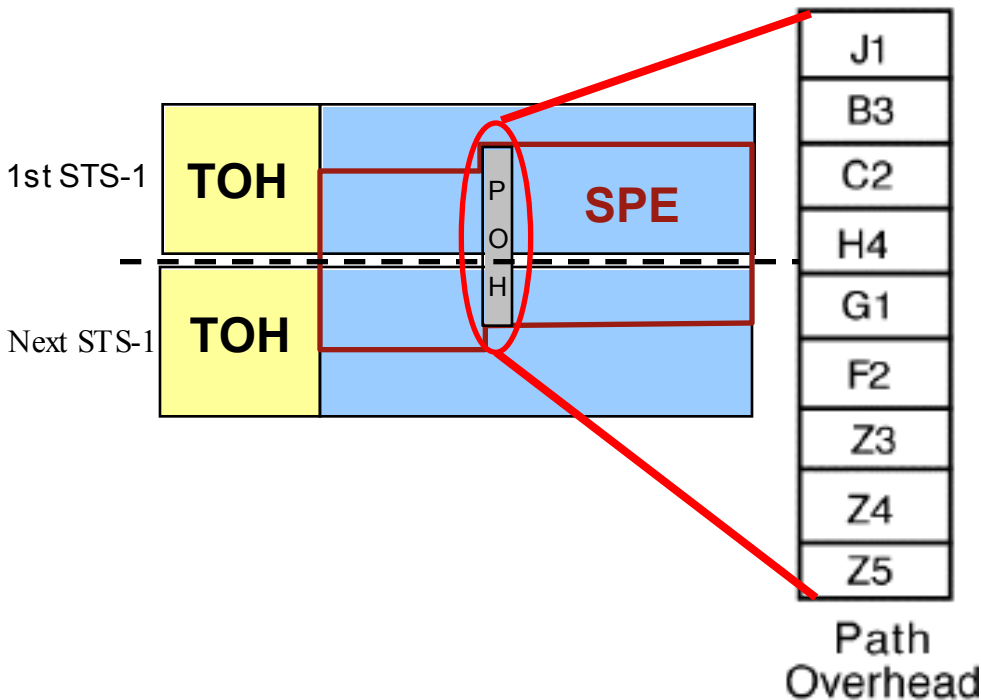
		1	2	3
Section Overhead	1	A1	A2	J0/Z0
	2	B1	E1	F1
	3	D1	D2	D3
Line Overhead	4	H1	H2	H3
	5	B2	K1	K2
	6	D4	D5	D6
	7	D7	D8	D9
	8	D10	D11	D12
	9	S1/Z1	M0 or M1/Z2	E2
		Transport Overhead		

Line Overhead



- Last 6 Rows of TOH
 - 18 Bytes
- Main functions
 - Locating the SPE in the frame
 - Muxing or Concatenating Signals
 - Performance monitoring
 - Automatic Protection Switching
 - Line Maintenance

Path Overhead



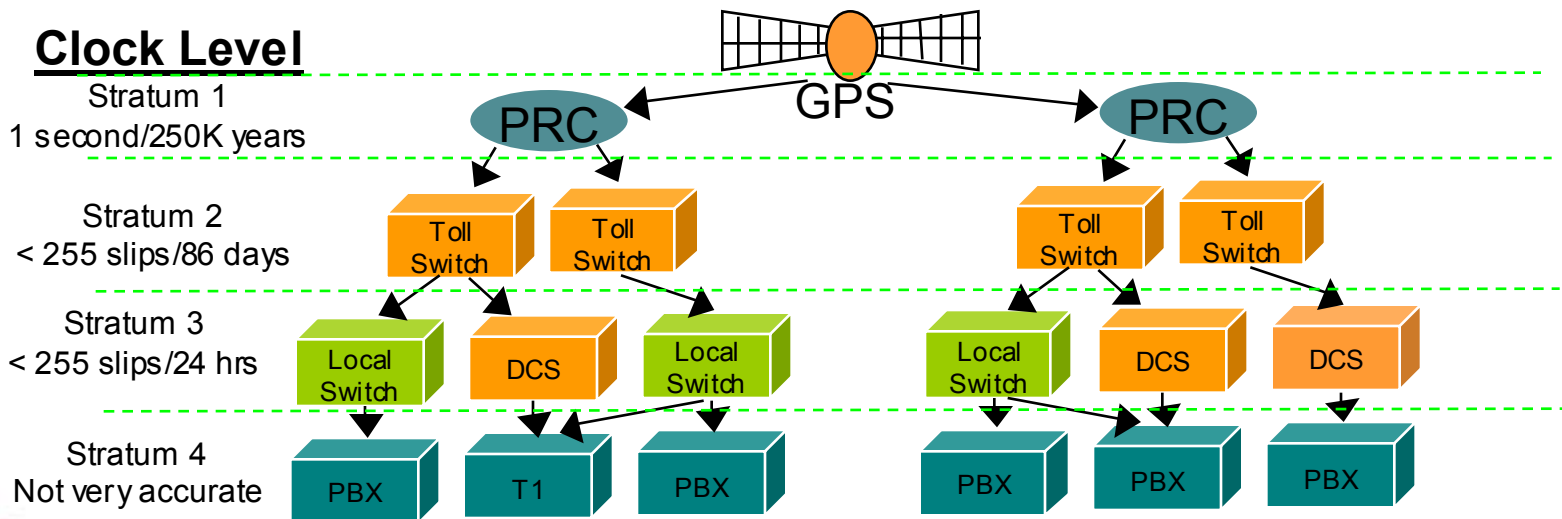
- 1st Column of the STS SPE is Path Overhead
 - an SPE can begin anywhere in the STS-1 envelope and overlap the adjacent frame.
- Main functions
 - Performance monitoring
 - Signal label, I.e. STS SPE content, including status of mapped payloads
 - Path status
 - Path trace

Alarms

- Various types of Alarms contained within the SONET overhead bytes to communicate an anomaly, defect or failure
 - Loss of signal
 - Loss of pointer, frame alignment
 - Remote error, defect, or failure Indication
 - Parity Errors
 - Loss of sequence synchronization
 - Alarm indication signal

SONET Synchronization

- Tiered timing model defines “stratum” levels
 - GPS timing propagates from stratum 1 Primary Reference Clocks (PRC) all the way down to stratum 4 Toll Switches
- Less accurate timing for higher Stratum values



SONET Synchronization

- Key features of SONET synchronization
 - SONET clocks are Stratum 3 accuracy or better
 - “Pointer adjustment” compensates for +/- 1 byte maximum offset for SONET by recalibrating start of SPE pointer as needed
- Not perfectly synchronous, but synchronous enough such that “bit stuffing” is not necessary
 - “Bit-stuffing” can lead to waste of bandwidth such as in the case of multiplexing DS-3s into a DS-4 where as much as 5 Mbps of bandwidth are lost due to “bit-stuffing”

SONET Traffic Types

- Virtual Tributaries
 - Voice channels
 - Data Traffic with rates less than DS-3
 - T1/E1 inclusive
- DS-3
- ATM Cells
 - SONET used as the B-ISDN transport
- Packet over SONET (POS)
 - Any layer 3 packet, but almost always IP

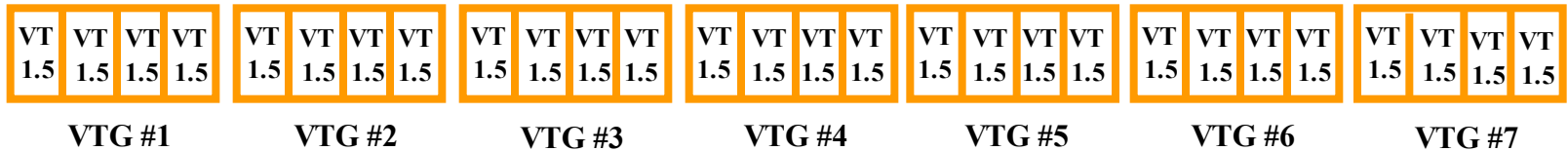
Virtual Tributaries (VT)

- SONET allows efficient transport and accessibility to lower rate signals by defining Virtual Tributaries in an STS-1
- Value of 02H in C2 POH bytes tells receiver that the arriving SPE contains VT signals
- 7 virtual tributary groups (VTG) each with 12 columns
 - $12 * 7 = 84$ columns of the 87-column STS-1 SPE
- Each VTG carries one type of the four Virtual Tributary types

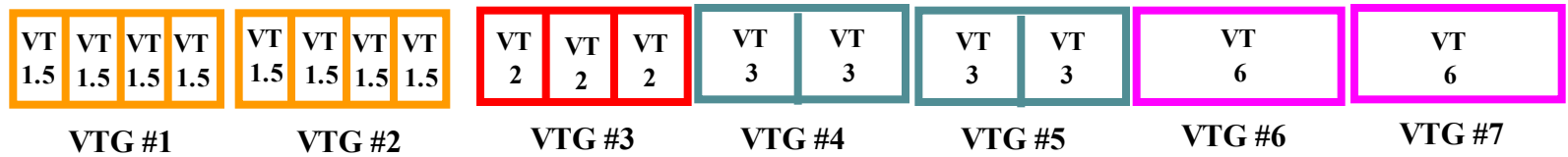
VT Type	Bitrate	Size of VT
VT 1.5	1.728	9 Rows, 3 Columns
VT 2	2.304	9 Rows, 4 Columns
VT 3	3.456	9 Rows, 6 Columns
VT 6	6.912	9 Rows, 12 Columns

VT Mapping

CASE1: All VTGs are VT1.5 Types



CASE2: 2 VT1.5, 1 VT2, 2VT3, 2 VT6



- Flexible VTG mapping within the STS-1 SPE
- Note that VTGs are represented above as being in block sequence for ease of conceptualization
- Actual physical configuration in the SPE is that of interleaved columns from each VTG group

Other VT Features

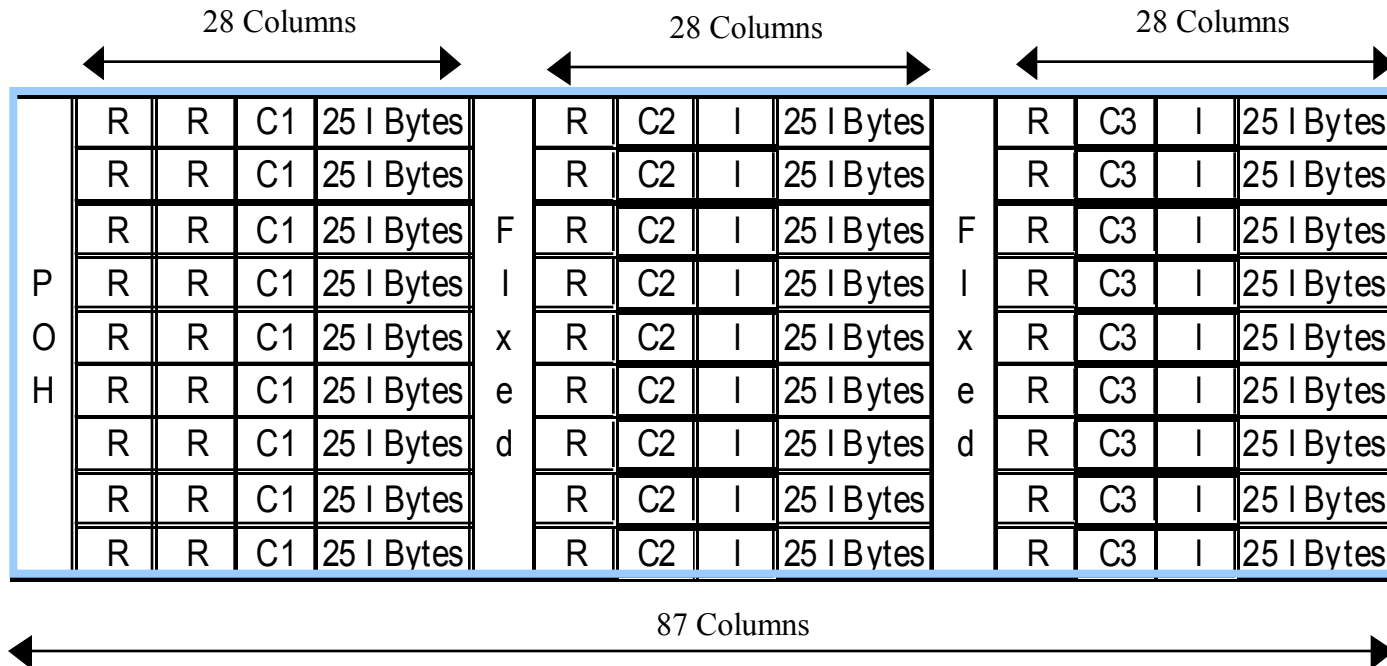
- VT Overhead
 - VTs have overhead similar in purpose to POH
- VT Mapping Modes
 - Locked mode
 - Fixed byte-oriented mapping
 - Not flexible
 - Floating Mode
 - Use of pointers allows payload to float with the VT payload capacity
 - Byte synchronous floating mode allows access to DS-0s

DS-3 Traffic

- DS-3 (channelized or unchannelized) transported in STS-1 SPE
- Value of 04H in C2 POH bytes tells receiver that the arriving SPE contains an asynchronous DS-3 signal
- No direct access to the DS-1s or DS-0s
- Best utilized when transporting DS-3s for long distances

DS-3 SPE

- 75 Columns of data (I Bytes) + 9 additional columns of Overhead (R, I, C1, C2, C3) besides POH and Fixed

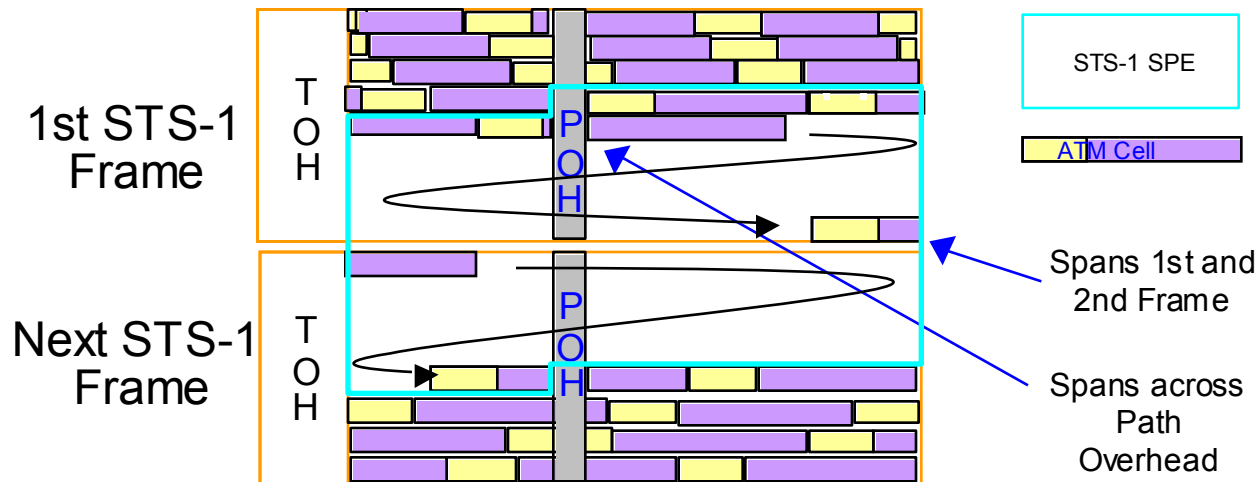


ATM Cell Transport

- ATM is the international standard for cell relay technology and together with SONET enable B-ISDN systems
 - ATM provides high speed switching while these high speed SONET links interconnect ATM switched networks
- Small, fixed sized- ATM Cells can be densely packed into an STS-1 with no additional SPE overhead aside from the POH; cell delineation done by the ATM switch

STS-1 SPE w/ ATM Cells

- 774 usable bytes (86×9) in an STS-1 SPE
- $774/53 = 14.6 \Rightarrow 14$ complete ATM cells/SPE
- Cells can have data or be idle (no information)
- ATM cells are mapped row-wise into the SPE



ATM Cell Transport

- C2 POH bytes tells receiver that the arriving SPE contains ATM Cells (value = 13H)
- SONET equipment never look at ATM cell headers as this is a Switch's function which SONET equipment are not!

Packet over SONET (PoS)

- PoS involves the transport of Packets, usually IP, over a SONET SPE with row-wise mapping of packets
- No such thing as a packet over SONET as IP packets are first framed before being sent
 - Point-to-point protocol (PPP) or High-Level Data Link Control (HDLC) frames are typically used

Packet over SONET (PoS)

- Have alternative ways to send packets over SONET, but some issues
 - Packets mapped column-wise into a DS-0 or VT1.5 is not as efficient as PoS in terms of SPE utilization
 - IP over ATM has issue of additional overhead
 - PoS is roughly 20 Mbps more efficient than ATM over SONET

Why Not Send Packets Directly Over SONET?

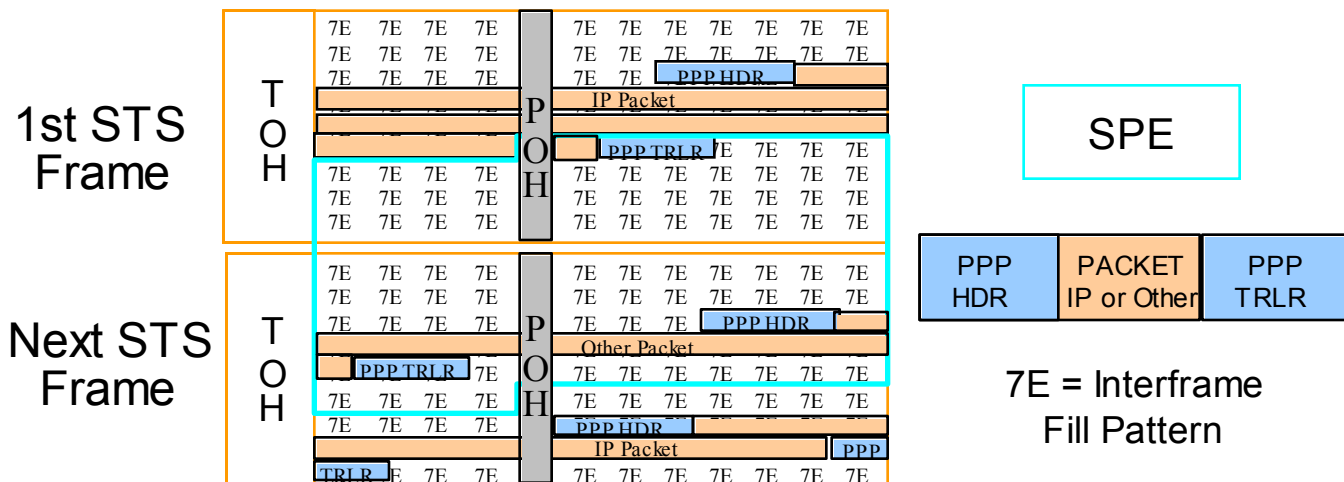
- Unlike a frame header/trailer, packet headers provide no error checking or at least inadequate error checking
 - Key to proper end-to-end transport of packets
- Frames provide good delineation of variable length packets
 - PPP & HDLC use interframe fill bit pattern (7Eh)
- Multiple Layer 3 packet types
 - Frames provide a way for a receiver to identify which packet type is in the frame (IP has 3 types)

HDLC and PPP for PoS

- HDLC considerations
 - Supported by SONET at STS-1, STS-3c (STM-1) and STS-12c (STM-4)
 - POH C2 Bytes = 16h tells SONET Mux that STS SPE contains HDLC frames
- PPP Considerations
 - Supported by SONET at STS-1, STS-3, STS-9, STS-12, STS-18, STS-24, STS-36, STS-48
 - Supported by SDH at STM-1, STM-4 or STM-16
 - POH C2 Bytes = CFh tells SONET Mux that STS SPE contains PPP frames

PoS SPE (Using PPP)

- Row-wise mapping of PPP frames into SPE
 - Same concept for HDLC version of PoS
- Frames are of variable length so could have any number within the SPE





SDH



Why Two Standards: SONET & SDH?

- The Plesiochronous Digital Hierarchies (PDH) line rates across the world all start at DS-0/E-0 level (64 kbps) but vary after that
 - NADH (N. America), JDH (Japan), EDH (Europe)
- Original SONET proposal did not accommodate all PDH systems
- SDH is essentially a SONET adjusted to accommodate the slight differences between NADH and the rest of the world's digital hierarchies

SDH vs. SONET

- SONET & SDH are more similar than different
 - SONET and SDH equipment are fully interoperable
 - SDH is the “international version of SONET”
- Differences are relatively minor:
 - Basic Frame size and line rate
 - Base SDH container, STM-1 (OC-3) is 3 times the size of SONET STS-1, i.e. 9 rows by 270 columns and 3 times the line rate, i.e. 155.52 Mbps

SONET vs. SDH

- Nomenclature differences
 - For example, Virtual Tributaries = Virtual Containers
 - Section = Regenerator Section, Line = Multiplex Section
- Some differences in overhead
 - C2 POH Payload byte mapping differs between SONET & SDH

SDH Line Rates

- SDH base line-rate is 155.52 Mbps STM-1
- Higher order line rates are multiples of STM-1

Electrical	SONET	Line Rate	SDH Equivalent
STS-1	OC-1	52 Mbps	-
STS-3	OC-3	156 Mbps	STM-1
STS-9	OC-9	467 Mbps	-
STS-12	OC-12	622 Mbps	STM-4
STS-18	OC-18	933 Mbps	-
STS-24	OC-24	1.2 Gbps	-
STS-36	OC-36	1.9 Gbps	-
STS-48	OC-48	2.5 Gbps	STM-16
STS-96	OC-96	5 Gbps	-
STS-192	OC-192	10 Gbps	STM-64
STS-768	OC-768	40 Gbps	-

STS = Synchronous Transport Signal
 OC = Optical Carrier
 STM = Synchronous Transport Module

- STM-1 is the ~~workhorse~~ for the SDH system
 - Typically for transport 139.264 Mbps PDH E-4

SDH Continues to Grow

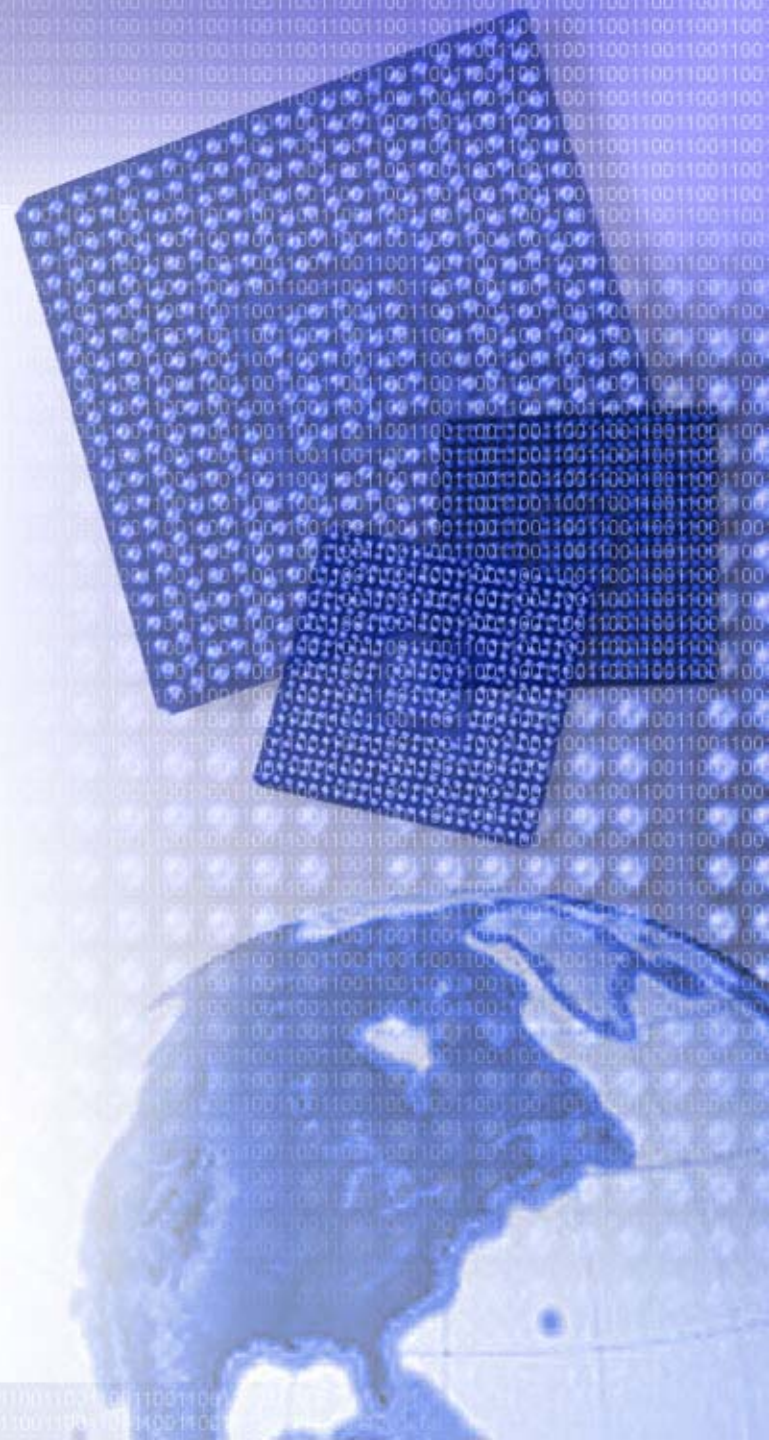
- SDH is the International Standard and SDH standards are used for international links
- Efforts for standardizing management systems for interoperable optical environments led by ITU
 - ITU defines standard for Telecommunications Management Networks (TMN)
- Demand for bandwidth has made OC-3 prevalent in U.S. which aligns well with STM-1

SDH Continues to Grow

- Equipment vendors tend to emphasize SDH over SONET to address the global standard
- SDH documentation which lagged SONET now stabilized
 - SDH networks can be installed and managed with confidence



SONET/SDH Equipment

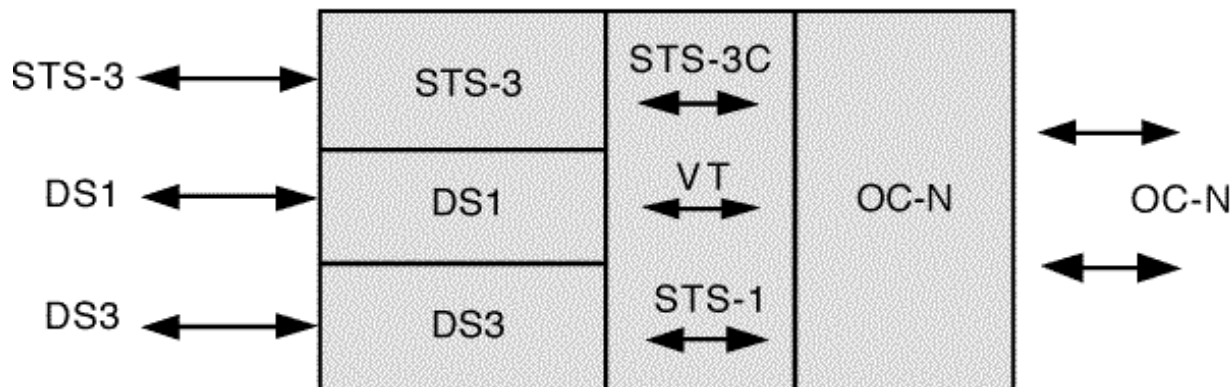


SONET/SDH Network Elements

- Terminal Multiplexer
- Add/Drop Multiplexer (ADM)
 - Matched Nodes
 - Drop and Repeat Nodes
- Digital Cross Connect (DCS)
- Regenerator
- Digital Loop Carrier (DLC)

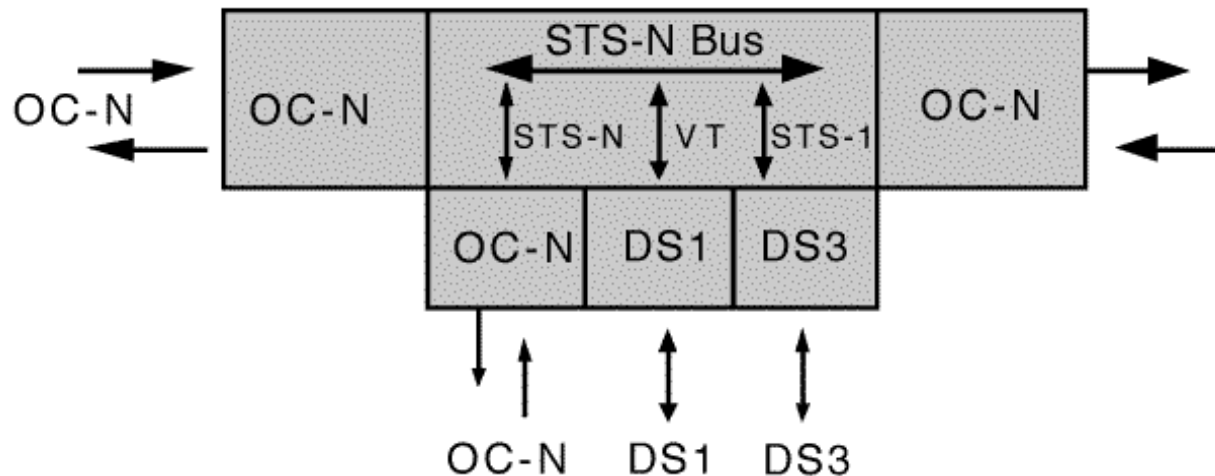
Terminal Multiplexer (TM)

- Basically combines PDH signals into an STS-N signal for transport onto an OC-N or disassembles an STS-N signal into lower rate PDH signals
- Almost always at the edge of a SONET/SDH network



Add/Drop Multiplexer (ADM)

- The ADM is the most prolific SONET/SDH equipment
- “Grooms” SONET STS-N, i.e. Add/Drop DS-n channels
- Allows access to transmission signals down to the DS-0 level without having to de-multiplex the whole SONET channel

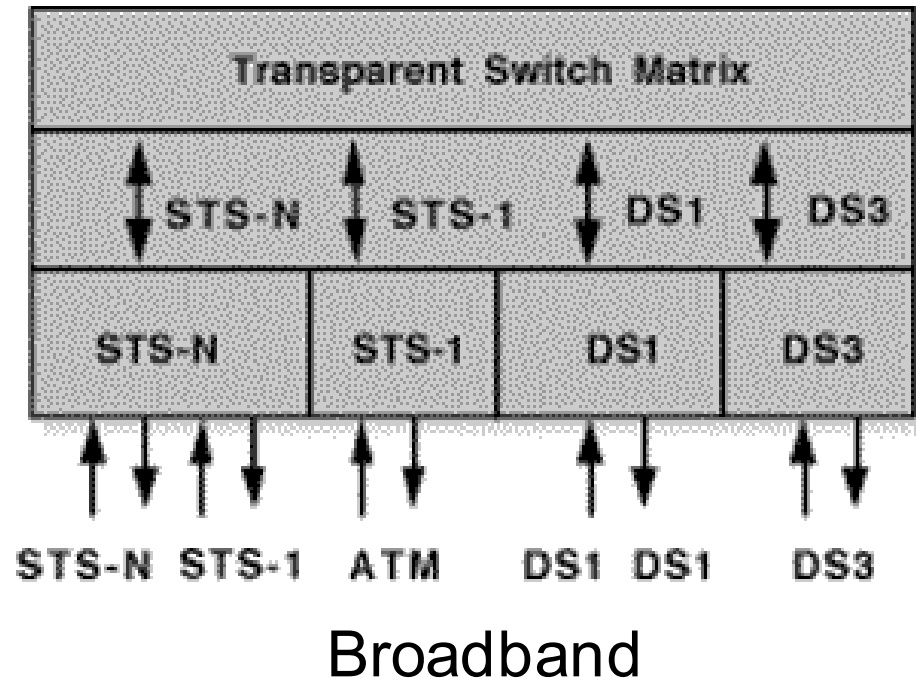


ADM Configurations

- SONET ADMs can be configured for specialized functions
 - Terminal Mode
 - As previously shown in the Terminal Multiplexer
 - Matched Node
 - Used when survivability of a inter-ring link is desired
 - Drop + Repeat Node
 - For broadcasting from a SONET/SDH ring (Cable TV)

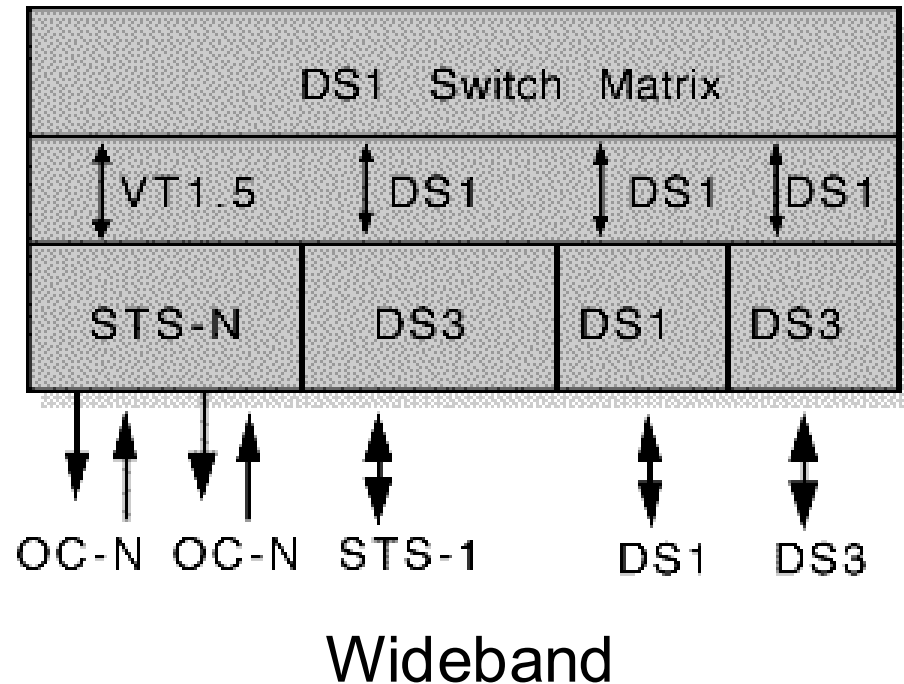
Broadband DCS

- A Broadband Digital Cross connect (DCS) accepts SONET rate signals, accesses STS-1 and switches at this level
- Also terminates DS1 and DS3
- Mainly used for STS-1 grooming and broadband traffic management



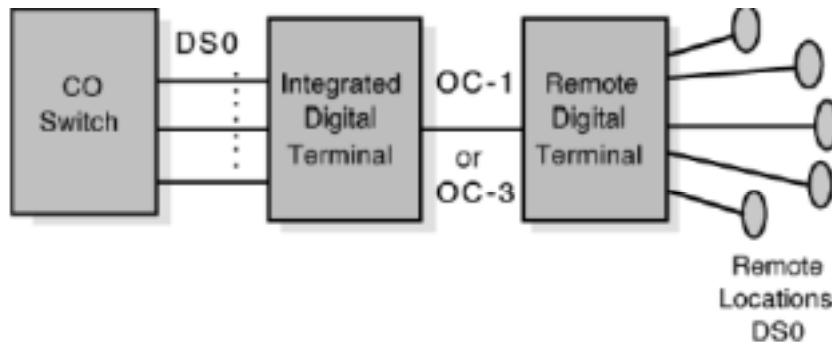
Wideband DCS

- Similar to Broadband DCS but switching is done at VT levels
- Mainly used for DS1 level grooming particularly at hub locations
- Use wideband DCS over DS3/1 cross connect to minimize mux/demux events

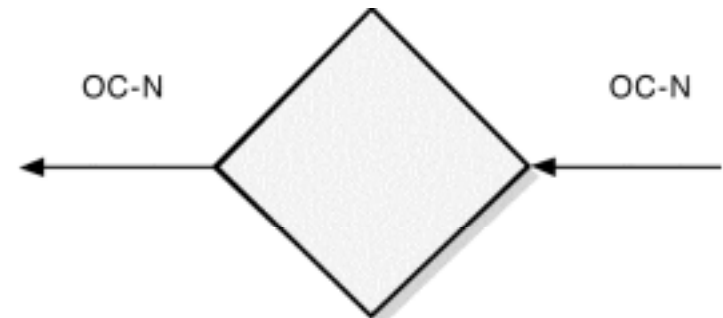


Other Equipment

- Digital Loop Carrier
 - Concentrates low-speed services before they are brought into the local Central Office for distribution
 - Economical when demand is in between 200 and 2000 lines



- Regenerator
 - Regenerates a signal weakened by attenuation over long distance
 - e.g, 1310nm optical signal needs regeneration every 26 mi.

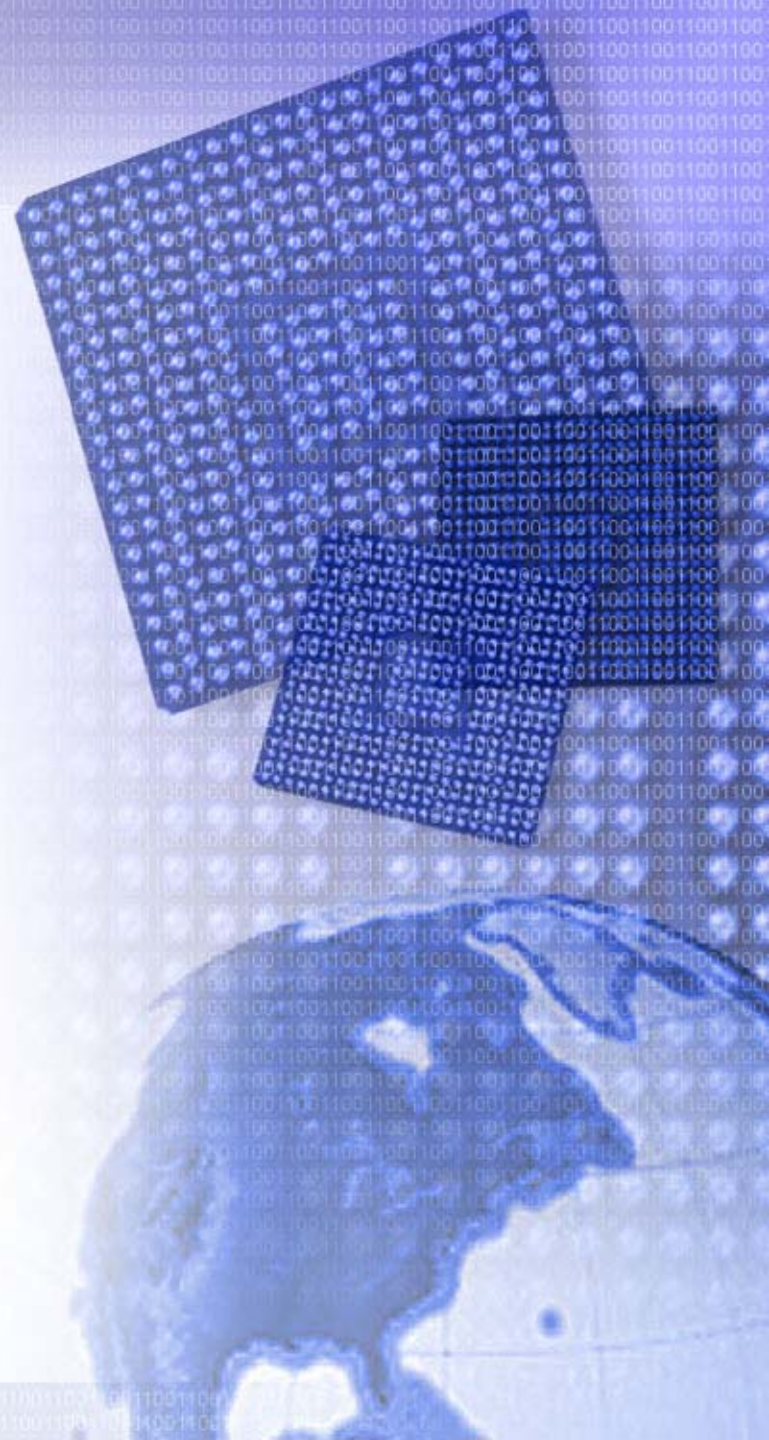


SONET Configurations

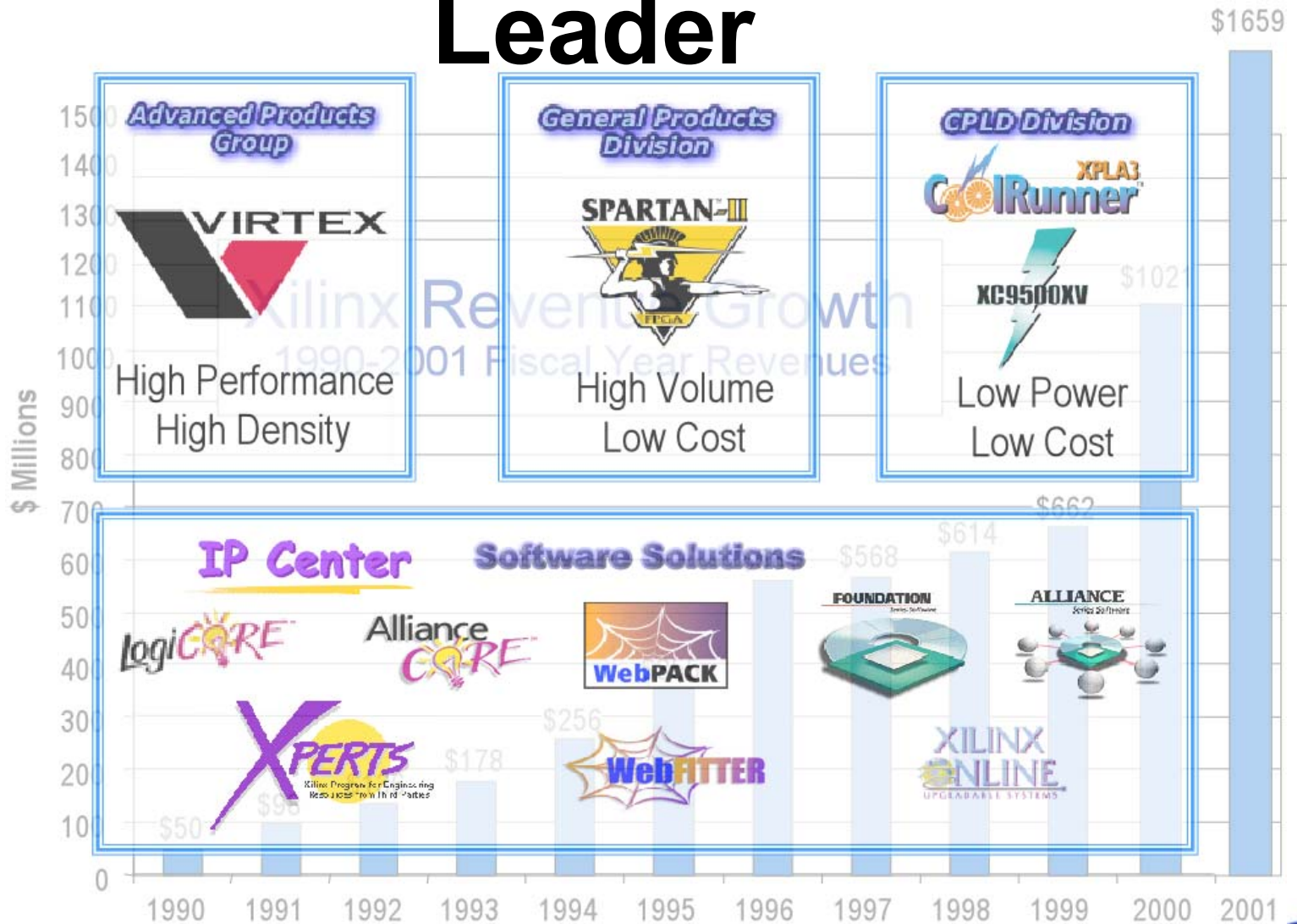
- 5 Basic Configurations
 - Point-to-point
 - Terminal Muxes linked by fiber
 - Point-to-multipoint
 - Terminal Muxes + ADMs along the way to pick up or drop off traffic to other points
 - Hub
 - Digital Cross Connect (DCS) serves as a hub
 - Ring
 - Most reliable and popular. More on this later
 - Mesh - More on this later



Xilinx Solutions

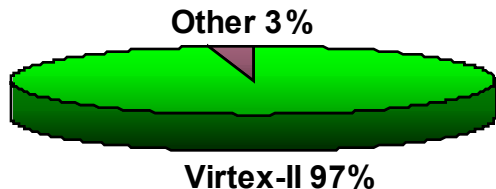


Xilinx – The PLD Industry Leader

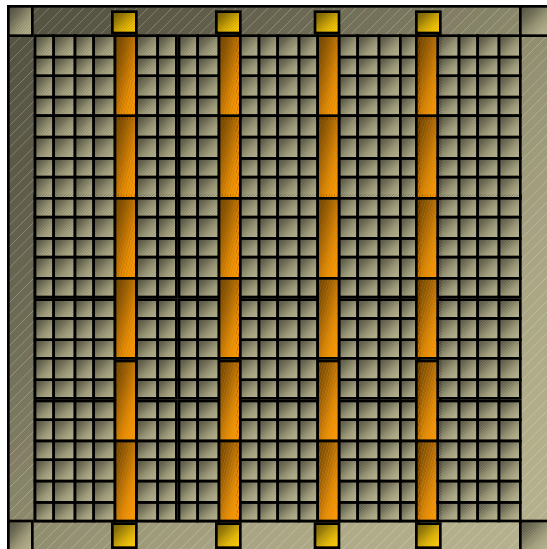


Virtex-II: The Winning Architecture

Advanced FPGA Market Share

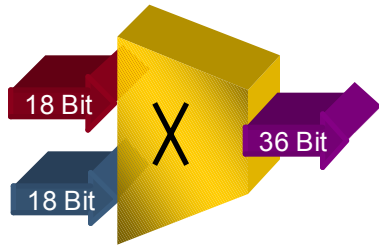


*Based on Q1-Q3 CY '01
market data for 1.5 V FPGAs*

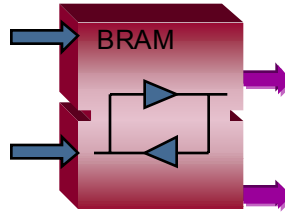


- #1 FPGA architecture
- 150 nm 8-layer metal CMOS
- Advanced logic & routing
- Highest density in the industry
- Embedded Dual Port RAM
- BlockRAM
- Xtreme DSP - multipliers
- DCM™
- XCITE technology - DCI
- SelectIO-Ultra™
- Triple DES security
- IP-Immersion™ technology

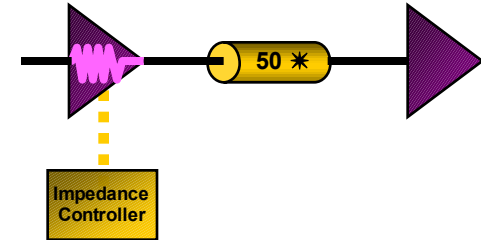
Virtex-II Features



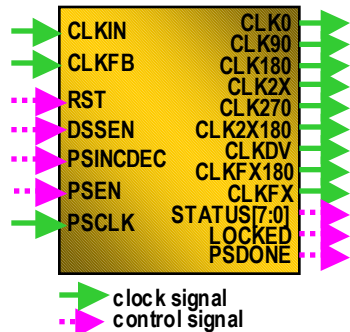
Embedded DSP functionality - up to 500 Billion MAC/s



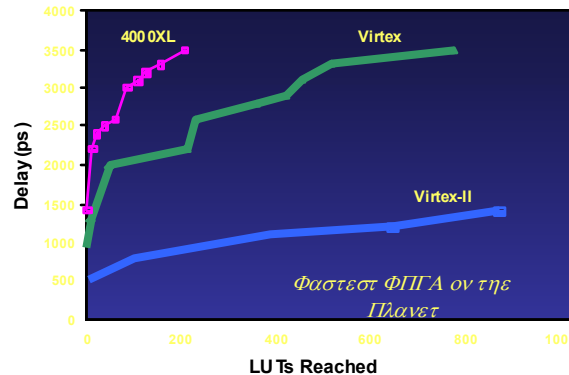
Embedded Dual-Port RAM - for Data Buffering



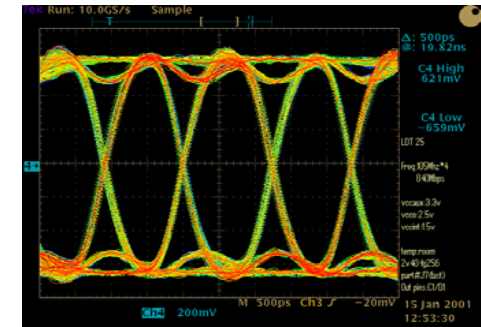
XCITE Digitally-Controlled Impedance (DCI) for simpler PCB layout



Digital Clock Management (DCM) - Precise Clock Generation



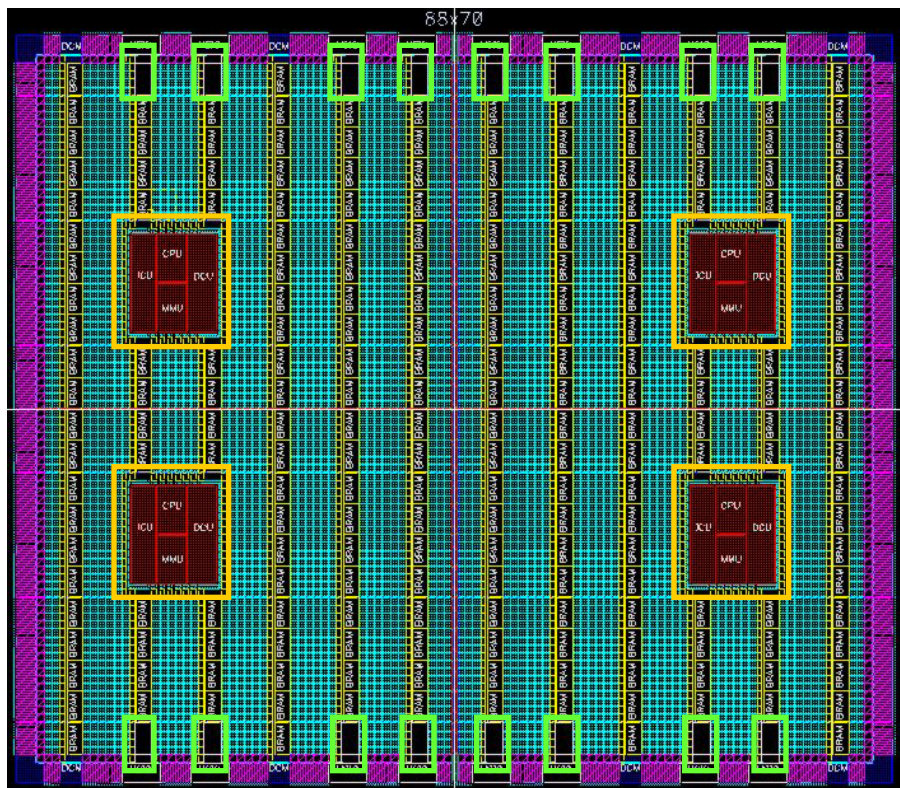
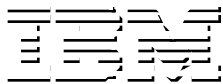
Active Interconnect Technology with a 300 MHz System Clock



SelectIO™ 25 IO types including 840 Mbps LVDS

Virtex-II Series Expanded to Include Virtex-II Pro

MNDSPEED™
A CONEXANT BUSINESS



- Virtex-II Logic, Routing, Features
 - Upward compatible, same design tools
 - Embedded Multipliers, SelectIO-Ultra (with 840Mbps LVDS), DCI/XCITE, DCM
- Up to 24, 3.125 Gbps serial transceivers
 - Channel bonding, 8b/10b encoding
 - Supports high-speed interfaces GbE, 10GbE (XAUI), PCI/PCI-X, Infiniband, RapidIO, HyperTransport, FlexBus 3/4, POS-PHY 3/4
- Up to four IBM 405 PowerPCs[®]
 - 32-bit RISC CPU: 420 DMIPS @ 300 MHz
 - The leading embedded CPU architecture in telecom & networking infrastructure
 - IBM CoreConnect™ on-chip bus

SystemIO

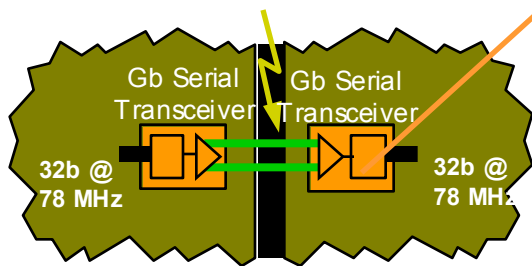
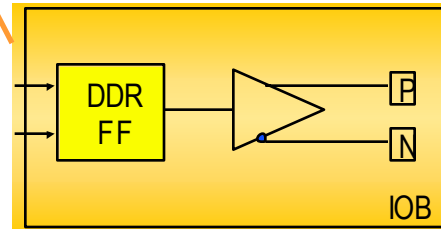
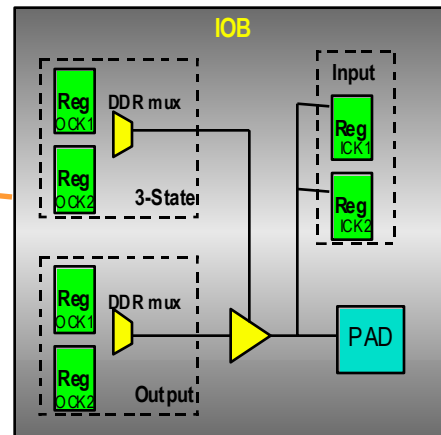
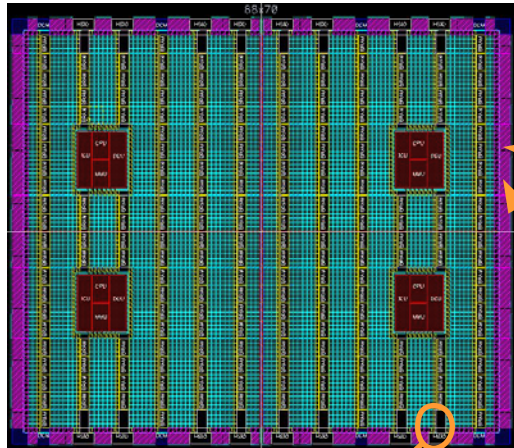
EmPower!

Virtex-II Pro and IP Solutions will Further Enable Next Generation Networking and Telecom Products

esp
EMERGING STANDARDS
& PROTOCOLS



Virtex-II Pro Helps You Manage the Transition from Parallel to Serial I/Fs



Rocket I/O Multi-Gigabit Serial Transceivers

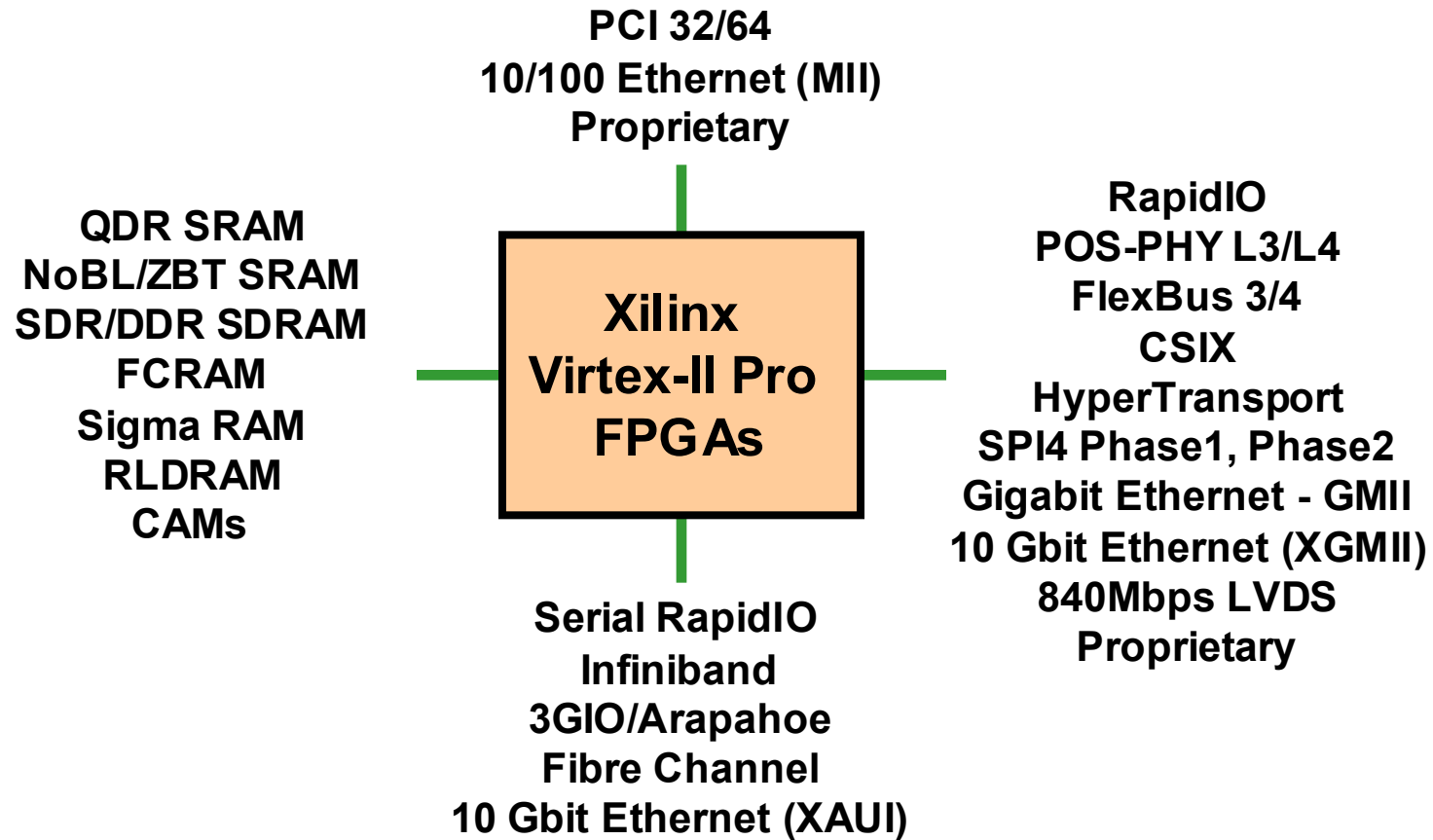
Up to twenty-four 3.125 Gbps transceivers

SelectI/O-Ultra™ technology for parallel interfaces

- 25 I/O Standards
- XCITE Technology
- 840 Mbps LVDS
- Dedicated DDR Registers

- Helps preserve investment in legacy designs
- Eases transition from parallel to serial technology
- Parallel interface designs will not go away

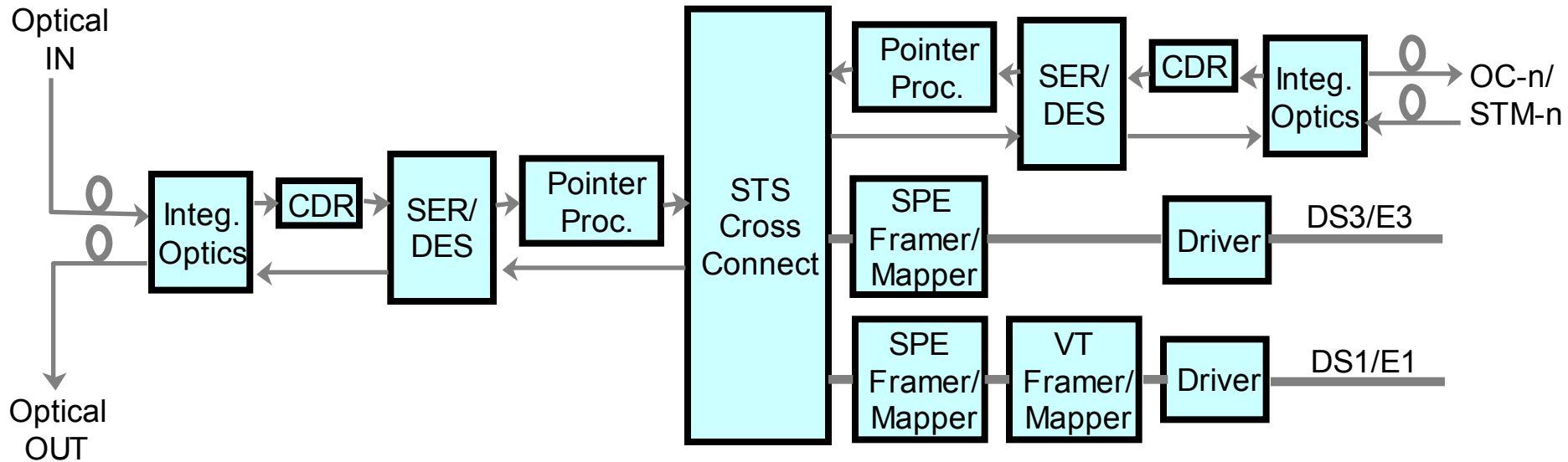
Supporting Legacy & Evolving System Interfaces



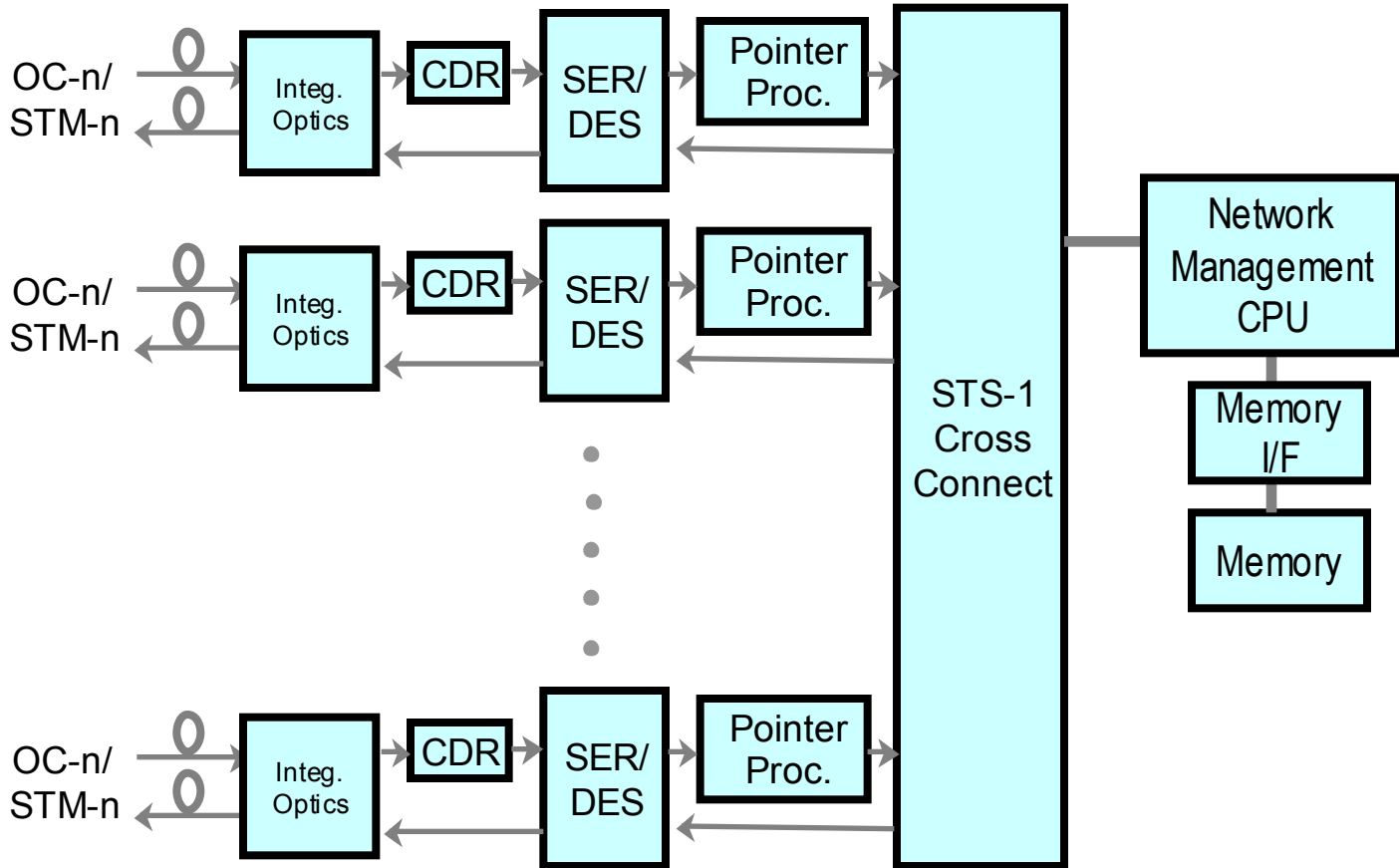
Optical Networking Related Soft IP Available Today

- Networking / Telecom
 - 1/10Gb Ethernet MACs - XAUI, XGMII
 - 10/100 Mbps Ethernet MACs
 - T1/E1 Framer/De-framer
 - UTOPIA Level-2/3 PHY-ATM
 - Network Classification Processor (2.5Gbps)
 - HDLC Controller
 - 8b/10b Encoder Decoder
 - Cell Assembler/Delineation
 - CRC10/32 Generator/Verifier
 - ADPCM 16 - 1024 channels
- 32-bit Xilinx Soft Processor: MicroBlaze
- 8-/16-bit Microcontrollers
- SystemIO Interfaces
 - RapidIO
 - PCI-X 64-bit / 100 MHz
 - PCI 32/33, PCI 64/66
 - SPI-3, SPI-4 P1/P2, FlexBus 3/4, POS PHY L3/L4, SFI-4
 - CSIX, HyperTransport, 3GIO, Fibre Channel, Infiniband
- High-Speed Memory Interfaces
 - SRAM - ZBT, QDR
 - DDR SDRAM
 - CAM
- Encryption
 - AES, DES, Triple DES

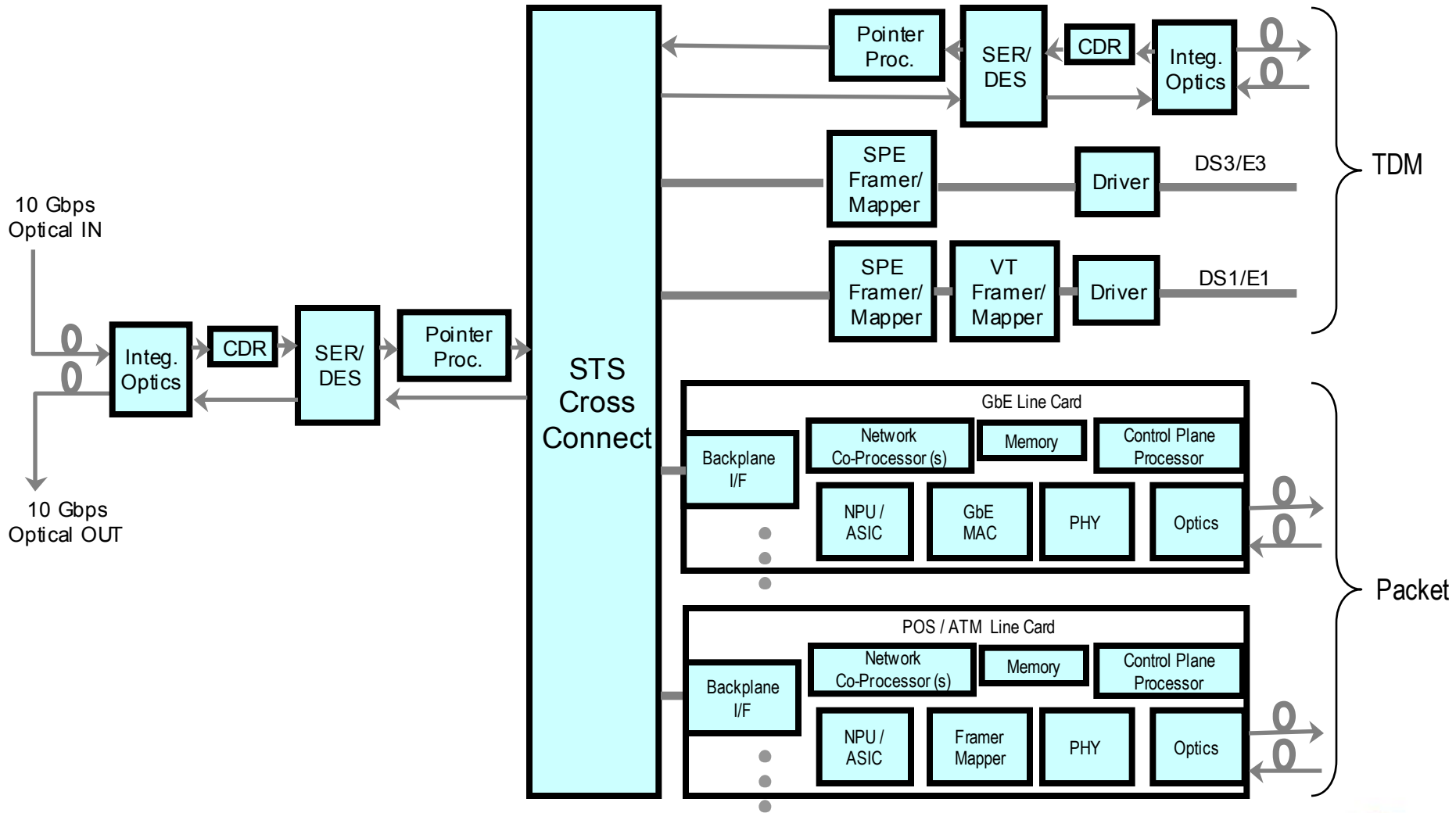
SONET ADM



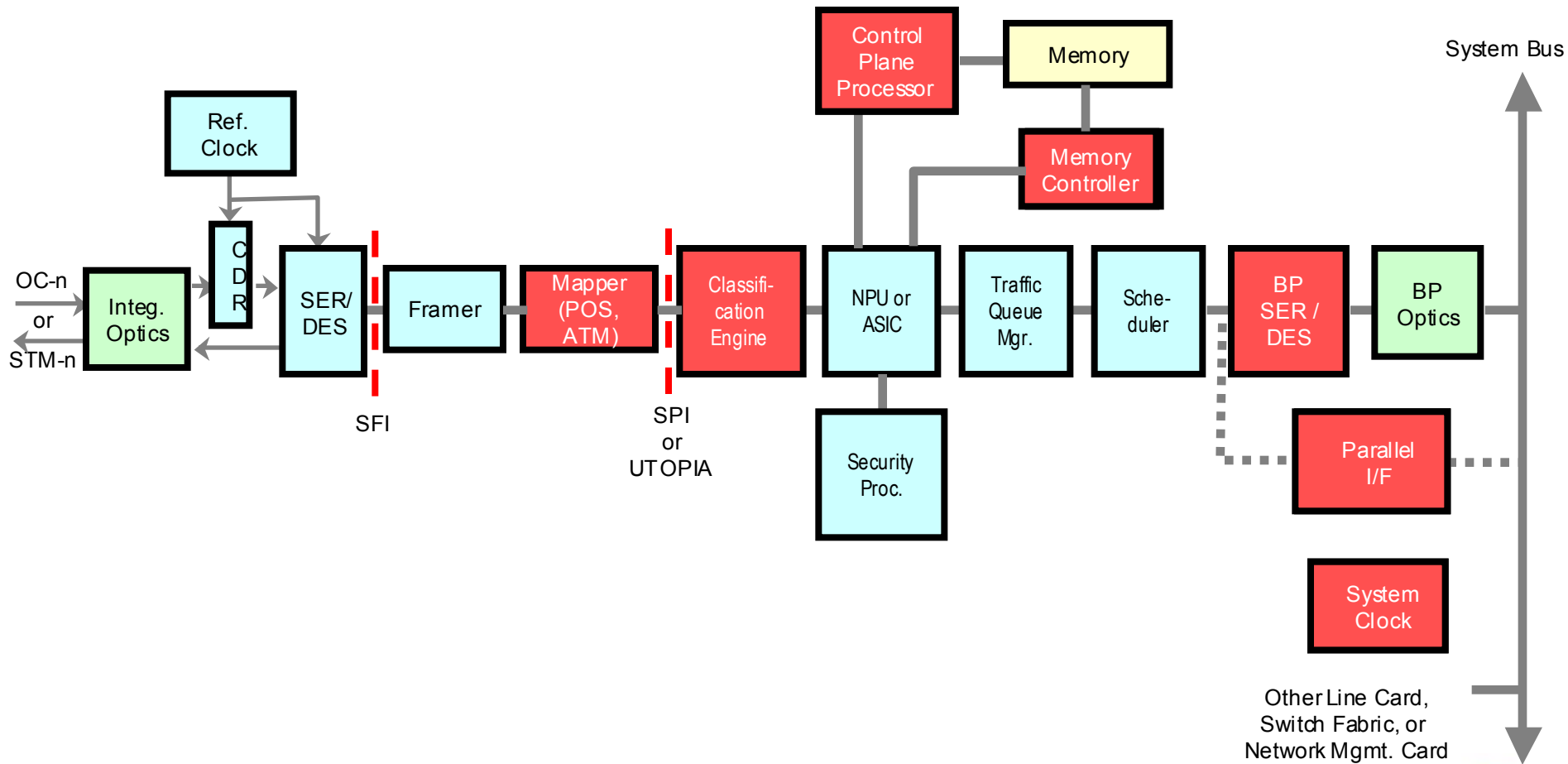
SONET DCS



SONET MSP



POS / ATM Line Card for SONET MSPP



Xilinx Solutions for SONET

- IP Cores
 - Interfacing IP Cores
 - PL3, PL4 / SPI 4.2, FlexBus 4 / SPI4.1, SFI 4, UTOPIA L2 / L3
 - Packet over SONET Cores
 - PPP8
 - HDLC Controller
 - IP over ATM Cores
 - ATM Cell Delineation and Assembly
- App Notes
 - 20-bit to 16-bit conversion (XAPP649)
 - “A1A2” Frame Bytes detection and Alignment (XAPP652)
 - SONET Scrambling (XAPP651)

PPP8, HDLC

- PPP8
 - Implements Point-to-point protocol encapsulation of packets
 - Supports 8-bit packet interface and PHY framer interface
 - Optimized for Virtex, Virtex-E, Virtex-II, Spartan-II
 - Conforms to RFC1619 PPP Over SONET specification
- HDLC Controller
 - Single-channel (HDLC1) and 32-channel (HDLC32) versions
 - Total data rate >40Mb/s with 32-channel version
 - Optimized for Virtex, Virtex-E, Virtex-II, Spartan-II
 - Compliant w/ ITU Q.921, X.25, ISO/IEC 3309, ISDN Ch. B & D
 - Competes with ASSPs as a cost effective HDLC solution



ATM Cell Assembly & Delineation

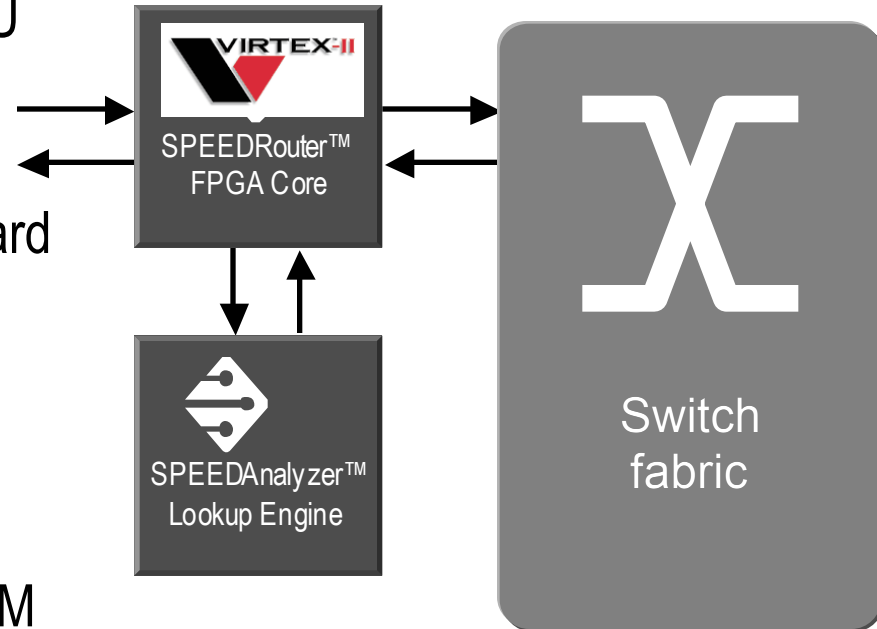


- Assembler IP
 - Performs the functions required in the transmit stream of the TC sub-layer of an ATM PHY processor
 - Conforms to SDH based specifications of ITU I.432.1.
 - Clock of up to 80 Mhz compatible w/ DS3, E3, STS-3c/12c
- Delineator IP
 - Performs the functions required in the receive stream of the Transmission Convergence
 - Conforms to SDH based specifications of ITU I.432.1.
 - Clock of up to 80 Mhz compatible w/ DS3, E3, STS-3c/12c

Classification Co-processing

- IP developed by IP Semiconductor
 - SPEEDRouter - Virtex-II FPGA
 - Full-duplex 2.5G FPGA based NPU
 - Programmable in Verilog using industry standard tool flow
 - Largest support for industry standard interfaces
 - SPEEDAnalyzer
 - VLIW uP lookup engine ASIC
 - Fully programmable
 - >1M entries with low-power SDRAM

**Alliance CORE
Member**



Interfacing IP

- UTOPIA

- Level 2: ATM-side and PHY-side IP Cores
- Level 3: ATM-RX, ATM-TX, PHY-RX, PHY-TX
- Fully compliant with ATM Forum UTOPIA specifications
- Single and Muti PHY support



- POS-PHY Level 3

- PHY-side and Link-side IP Cores
- SATURN and OIF SPI3 compliant
- Single & multi-PHY operation, scalable from 1 to 256 links
- 32-bit support for OC-48



Interfacing IP

- POS-PHY Level 4, Phase II
 - SATURN and OIF SPI-4 Phase II compliant
 - 16-bit data bus, 700 Mbps per LVDS pin pair
 - Single-link and multi-link operation
- Flexbus 4
 - AMCC Flexbus4 and OIF SPI4-01.0 compliant
 - 64-bit HSTL, 200 MHz
 - 1, 4, 16 channel configurations
 - Support for separate Rx and Tx functionality



Summary

- SONET/SDH's is the dominant optical technology in the PSTN & most high-speed Service Provider networks
- The legacy SONET/SDH equipment market is mature; next generation MSPP market shows high growth
- Xilinx suite of Silicon and IP provides solutions for legacy and emerging SONET/SDH systems
 - High-performance Virtex II fabric & features; addition of Power PC and MGTs on Virtex-II Pro
 - IP for Framers, System I/O, Memory Interfaces, Network processing



Questions?

For more information, go to:

Or contact the eSP team
espteam@xilinx.com

